

Compal Confidential

Huayra UMA (QCL51) Schematics Document

AMD Comal Platform

AMD Trinity APU / Hudson FCH / ATI Thames XT M2
Muxless/UMA / PX 5.0

2012-01-04

LA-8714P REV: 0.3

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				08	40191F	A
Date:				Tuesday, January 10, 2012	Sheet	1 of 54

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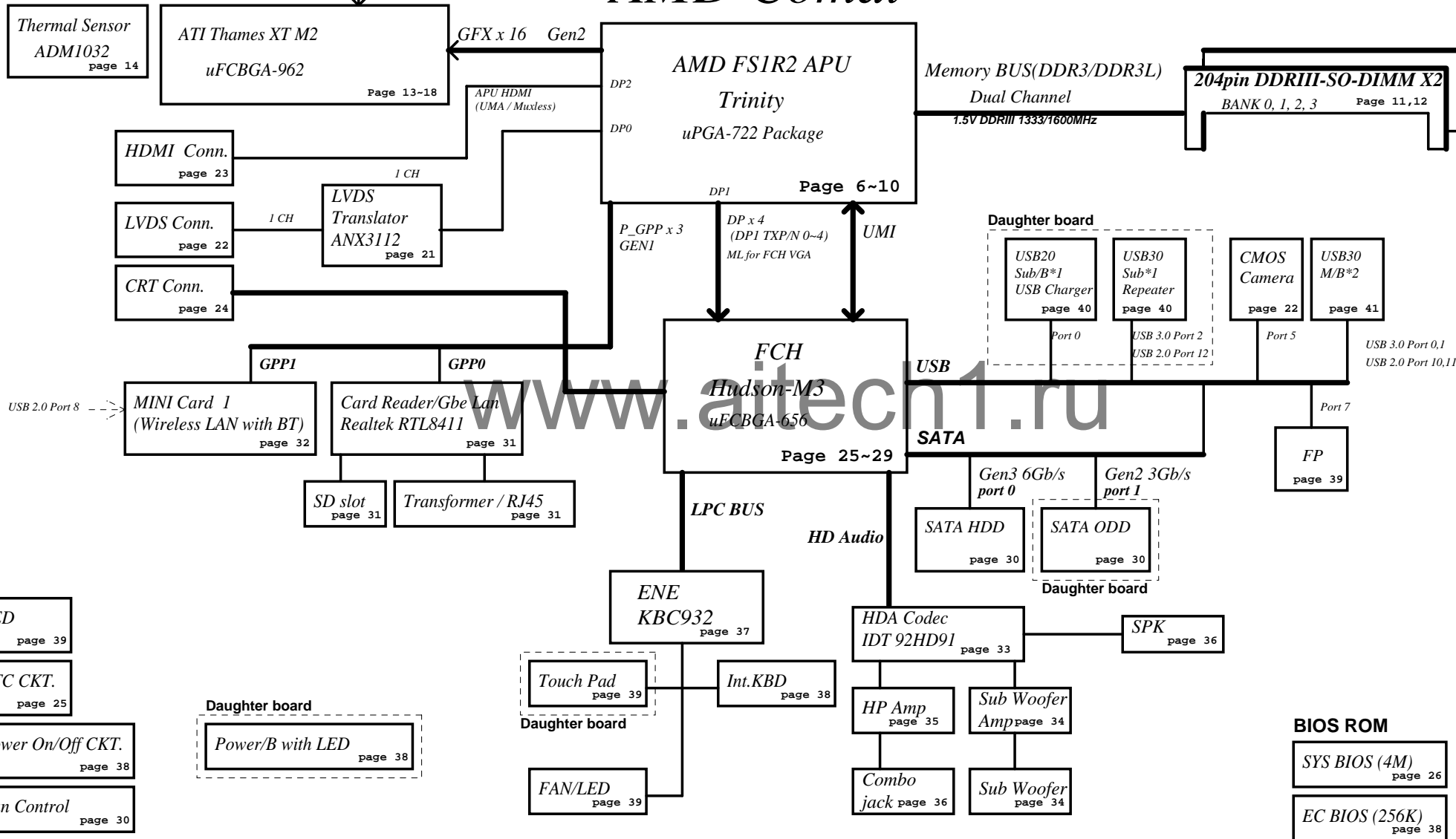
Model Name : QCL51 AMD

Board Name : LA-8712P

64M x16
128M x 16
VRAM DDR3
page 19, 20

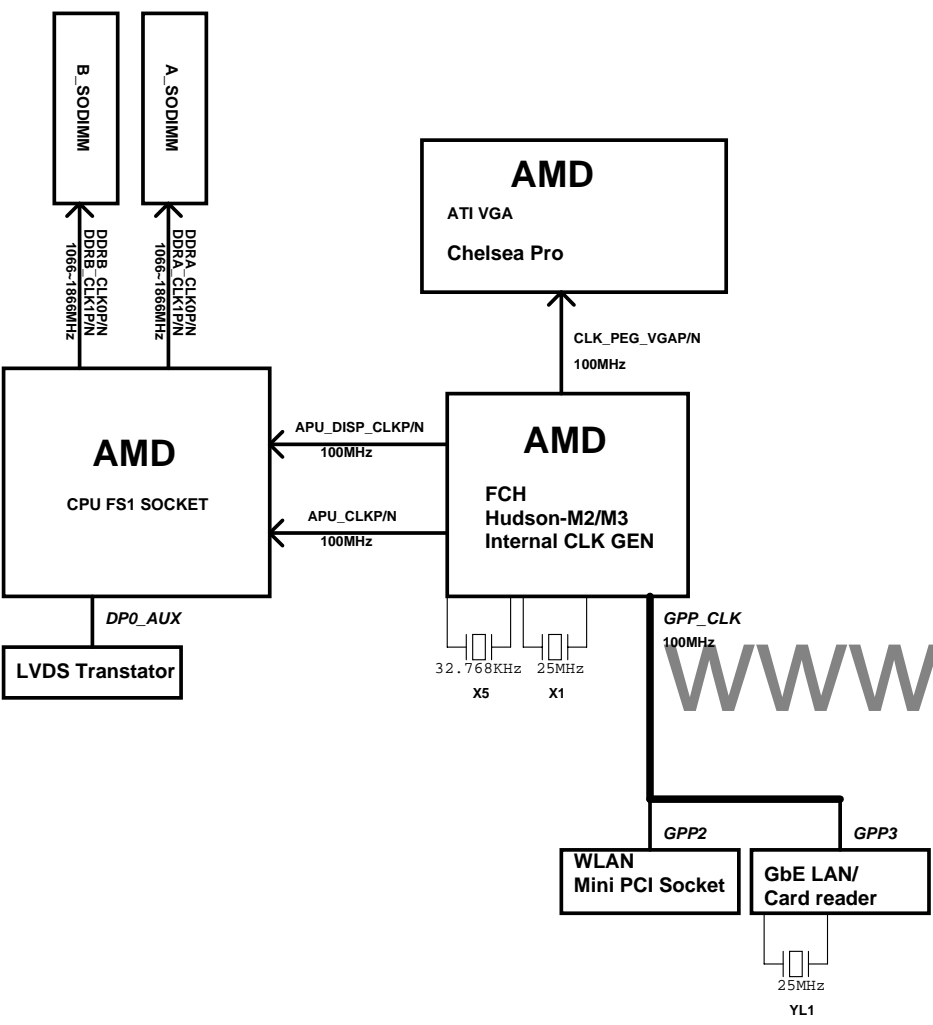
DDR3

AMD Comal

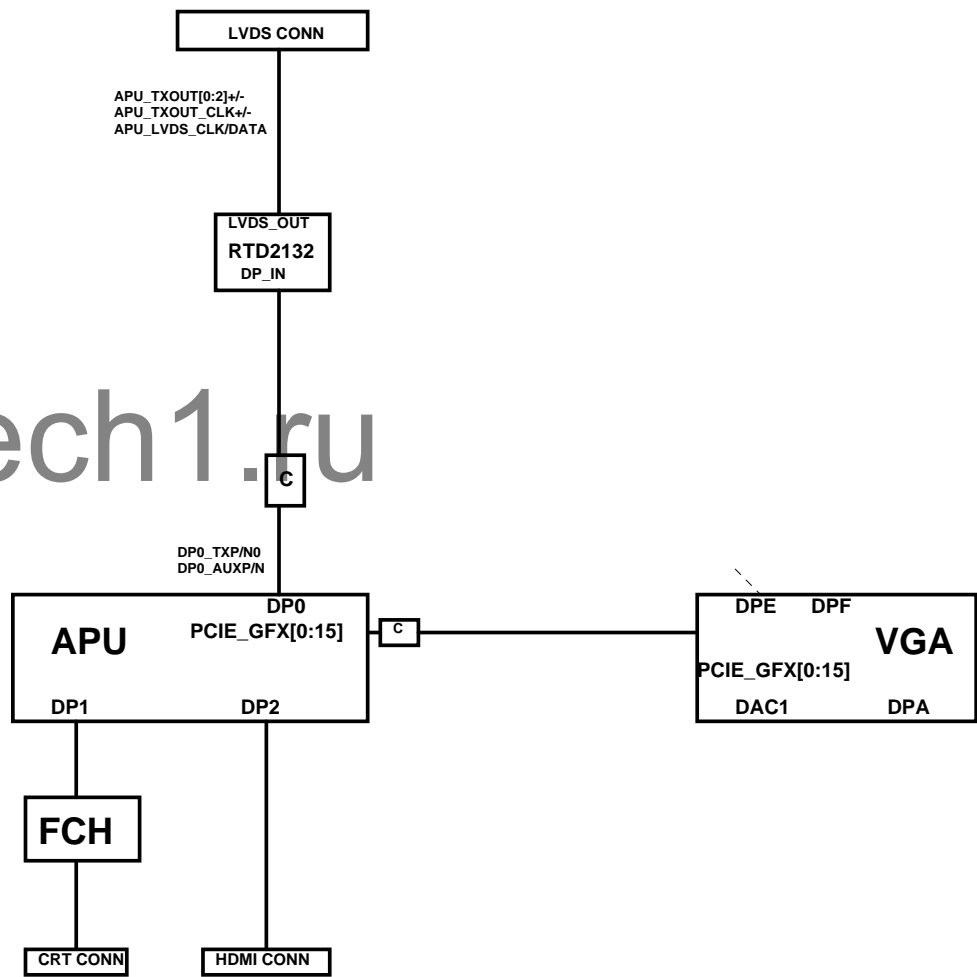


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Date:		Tuesday, January 10, 2012		Sheet		2		of		54	
										Rev A	

CLOCK DISTRIBUTION



DISPLAY OUTPUT



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				Date:	Tuesday, January 10, 2012
				Sheet	3 of 54
				Rev	A

Voltage Rails

Power Plane	Description	S1	S3	S5
VIN	Adapter power supply (19V)	N/A	N/A	N/A
B+	AC or battery power rail for power circuit.	N/A	N/A	N/A
+APU_CORE	Core voltage for CPU	ON	OFF	OFF
+APU_CORE_NB	Voltage for On-die VGA of APU	ON	OFF	OFF
+VGA_CORE	0.95-1.2V switched power rail	ON	OFF	OFF
+VDDCI	0.95-1.2V switched power rail	ON	OFF	OFF
+0.75VS	0.75V switched power rail for DDR terminator	ON	ON	OFF
+0.935VGS	0.935V switched power rail for VGA	ON	OFF	OFF
+1.1ALW	1.1V switched power rail for FCH	ON	ON	ON*
+1.1VS	1.1V switched power rail for FCH	ON	OFF	OFF
+1.2VS	1.2V switched power rail for APU	ON	OFF	OFF
+1.5V	1.5V power rail for CPU VDDIO and DDR	ON	ON	OFF
+1.5V_PCIE	1.5V switched power rail	ON	OFF	OFF
+1.8VGS	1.8V switched power rail	ON	OFF	OFF
+2.5VS	2.5V for CPU_VDDA	ON	OFF	OFF
+3VALW	3.3V always on power rail	ON	ON	ON*
+LAN_VDD_3V3	3.3V power rail for LAN	ON	ON	ON
+3VS	3.3V switched power rail	ON	OFF	OFF
+5VALW	5V always on power rail	ON	ON	ON*
+5VS	5V switched power rail	ON	OFF	OFF
+VSB	VSB always on power rail	ON	ON	ON*
+RTCVCC	RTC power	ON	ON	ON

Note : ON* means that this power plane is ON only with AC power available, otherwise it is OFF.

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3 (Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4 (Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5 (Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

Board ID / SKU ID Table for AD channel

Vcc	3.3V +/- 5%			
Ra/Rb	100K +/- 5%			
Board ID	Ra / Rb	VAD_BID min	VAD_BID typ	VAD_BID max
0	0	0 V	0 V	0 V
1	8.2K +/- 5%	0.216 V	0.250 V	0.289 V
2	18K +/- 5%	0.436 V	0.503 V	0.538 V
3	33K +/- 5%	0.712 V	0.819 V	0.875 V
4	56K +/- 5%	1.036 V	1.185 V	1.264 V
5	100K +/- 5%	1.453 V	1.650 V	1.759 V
6	200K +/- 5%	1.935 V	2.200 V	2.341 V
7	NC	2.500 V	3.300 V	3.300 V



DIS@
PCB
Part Number = DA80000SH00
PCB 00H LA-8712P REV0 M/B



UMA@
PCB
Part Number = DA60000T500
PCB 00H LA-8712P REV0 M/B

BOARD ID Table

Board ID	PCB Revision
0	DB
1	SI

BOM Option Table

BOM Structure	Description	DIS	PX@ DIS@ Tha@
PX@	PX function	UMA	UMA@
DIS@			
UMA@			
Tha@			

BOM Config

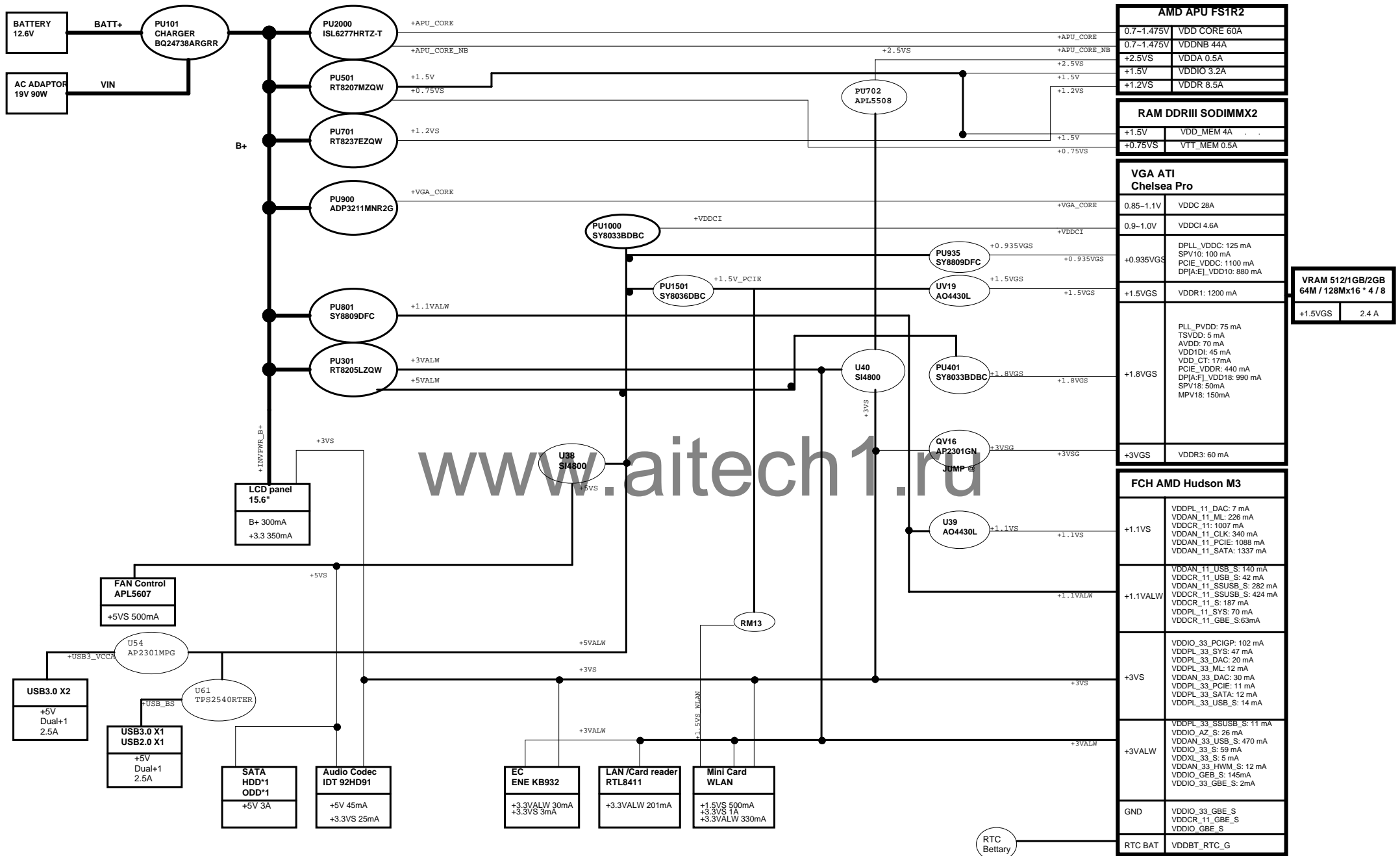
x = 1 is read cmd, x= 0 is write cmd.

Device	IDSEL#	REQ#/GNT#	Interrupts

EC SM Bus1 address			EC SM Bus2 address		
Device	Address	HEX	Device	Address	HEX
Smart Battery	0001 011X b	16H	ADI ADM1032 (GPU)	1001 101X b	9AH
			SB-TSI (APU)	1001 100X b	98H
			LVDS TR	1010 100X b	A8H
			VGA Internal Thermal	1000 001X b	82H

FCH (S0) SM Bus 0 address			FCH (S0~S5) SM Bus 1 address		
Device	Address	HEX	Device	Address	HEX
DDR DIMM1	1010 000X b	A0	Touch pad		
DDR DIMM2	1010 001X b	A2			
Amplifier					

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				Date:	Tuesday, January 10, 2012	Sheet 4 of 54



GPU

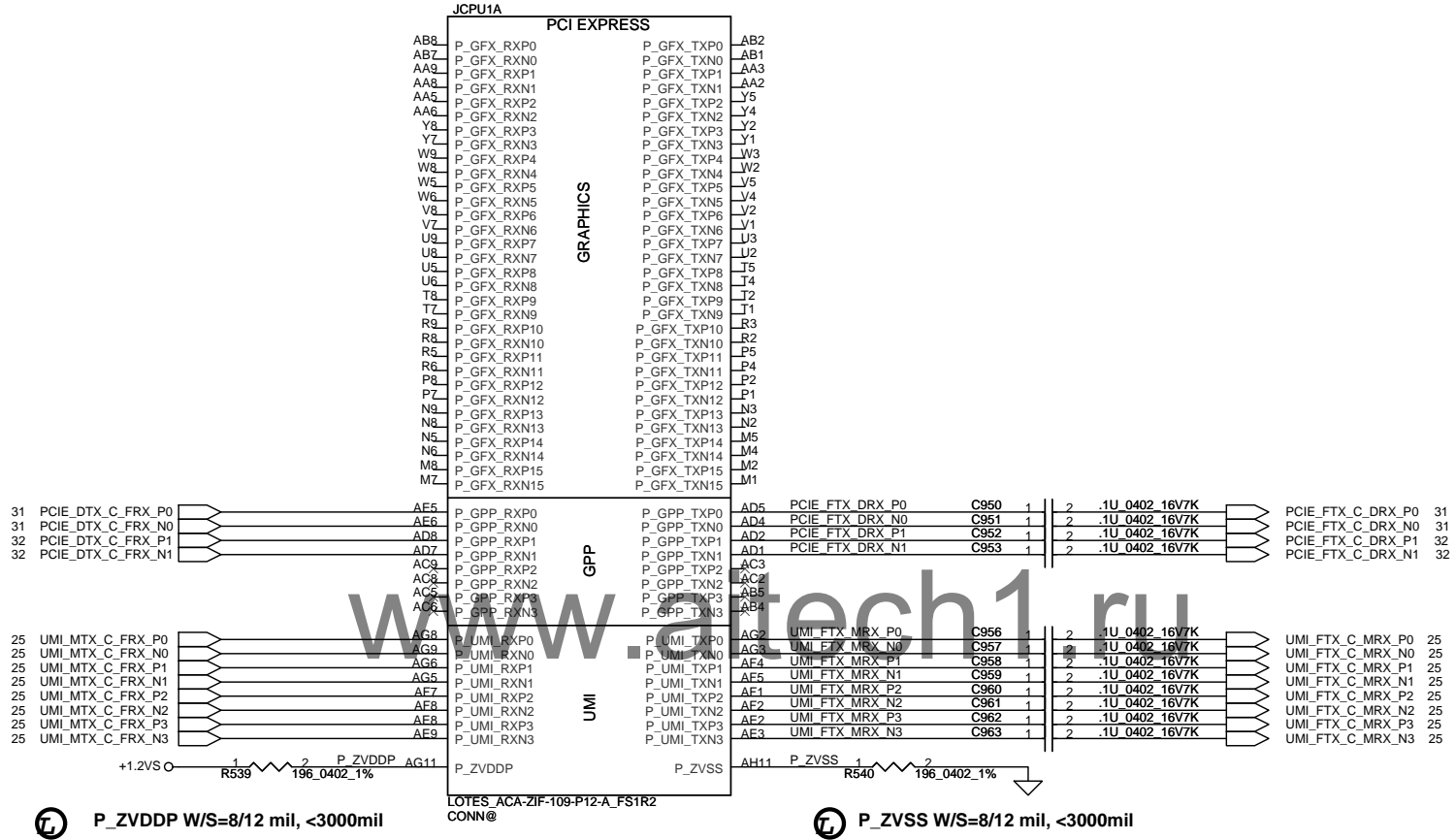
GLAN/Card reader
WLAN

UMI

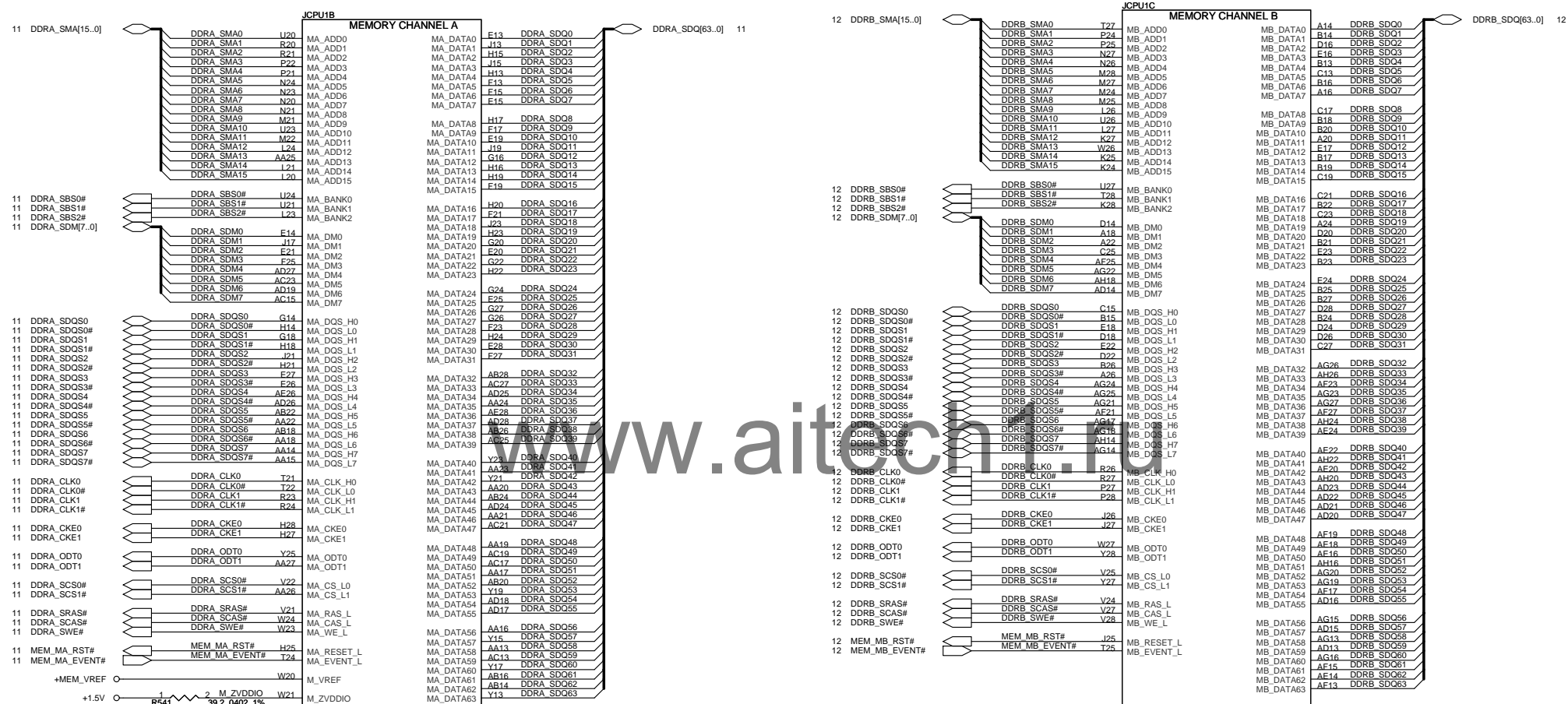
GPU

GLAN/Card reader
WLAN

UMI



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										SCHEMATICS, MB A8714	
										Document Number	
										4019IF	
										Date: Tuesday, January 10, 2012	
										Sheet 6 of 54	



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				Document Number	40191F
				Date	Tuesday, January 10, 2012
				Sheet	7 of 54

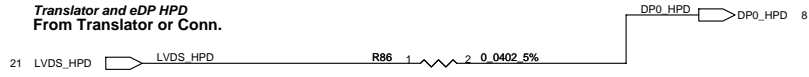
Power Name	Consumption
VDD +CPU_CORE	60A
VDDNB +CPU_CORE_NB	37A
VDDIO	3.2A
VDDP / VDDR	5A / 3.5A
VDDA	
+2.5VS	0.75A



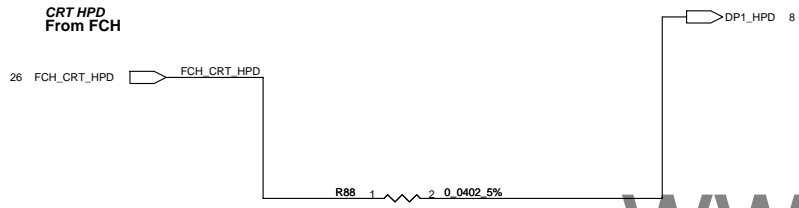
Pop / @	330uF	220uF	47uF	22uF	10uF	4.7uF	0.22uF	0.01uF	3300pF	1nF	180pF
Pumori 2.0			0	19/11	7	5	17	3	1	1 / 1	13/3
Comal	7 / 2	1	1	19/11	7	4	17	3	1	1 / 1	14/2
P5WS5	7 / 2	1	1	13	3	8	19	3	1	4	16

HPD

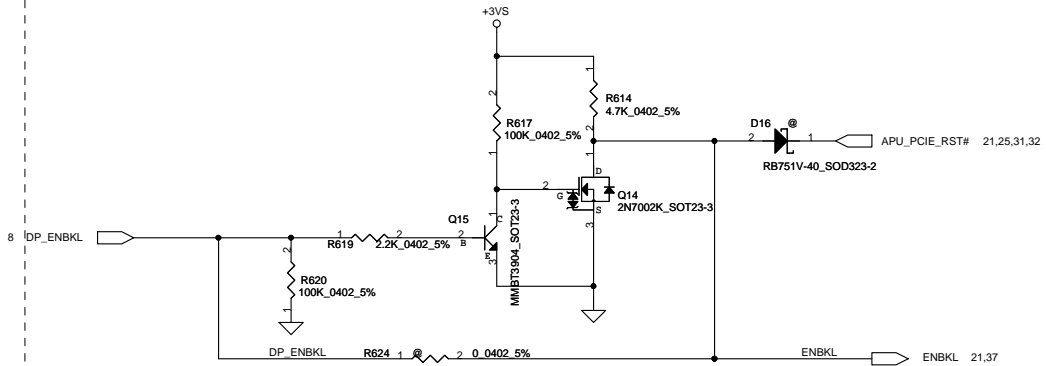
Translator and eDP HPD
From Translator or Conn.



CRT HPD
From FCH

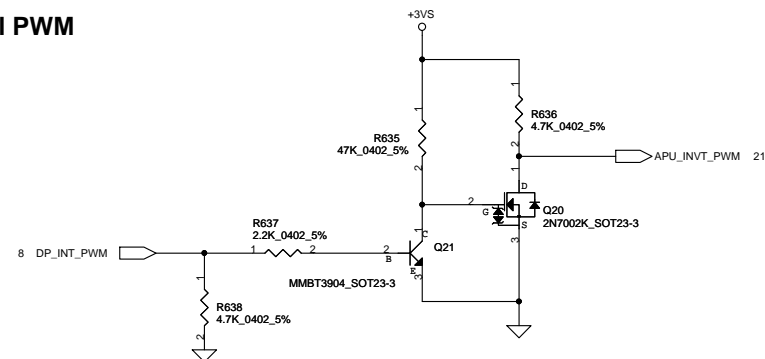


Panel ENBKL

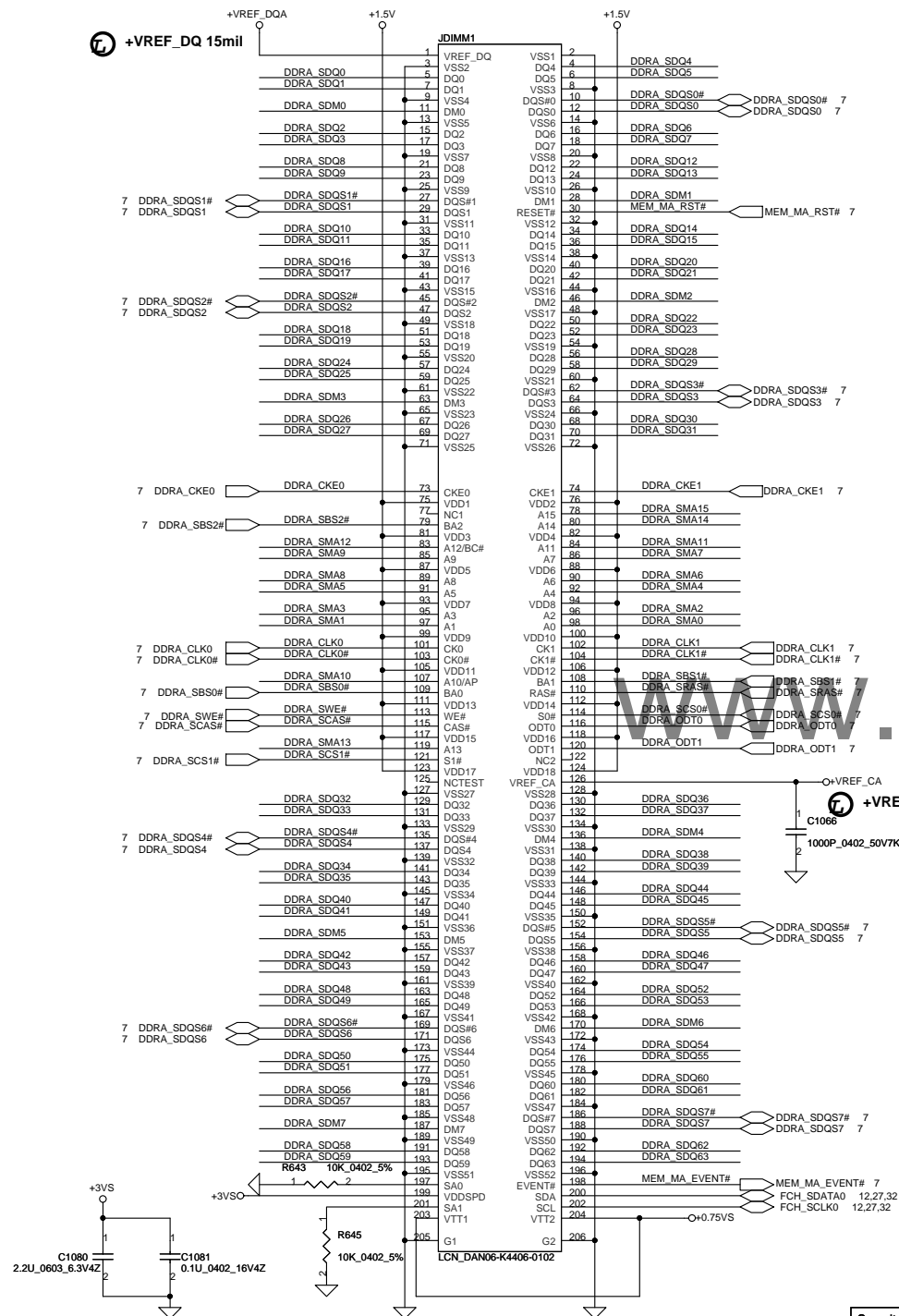


eDP Panel ENVDD

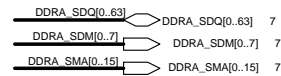
Panel PWM



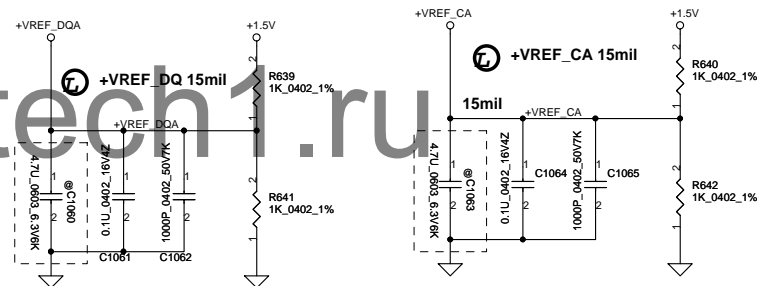
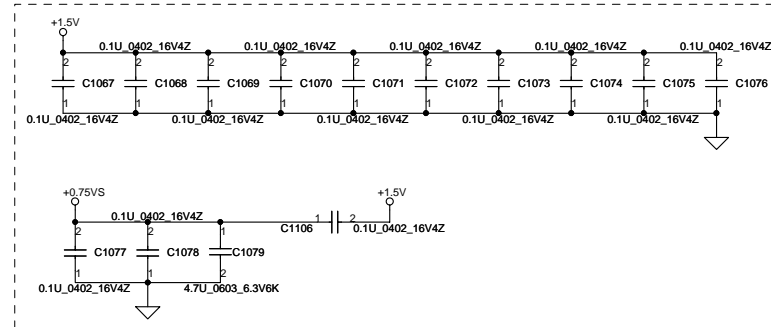
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						Document Number				Rev	
						4019IF				A	
						Date: Tuesday, January 10, 2012				Sheet 10 of 54	



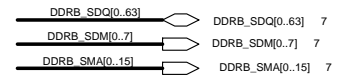
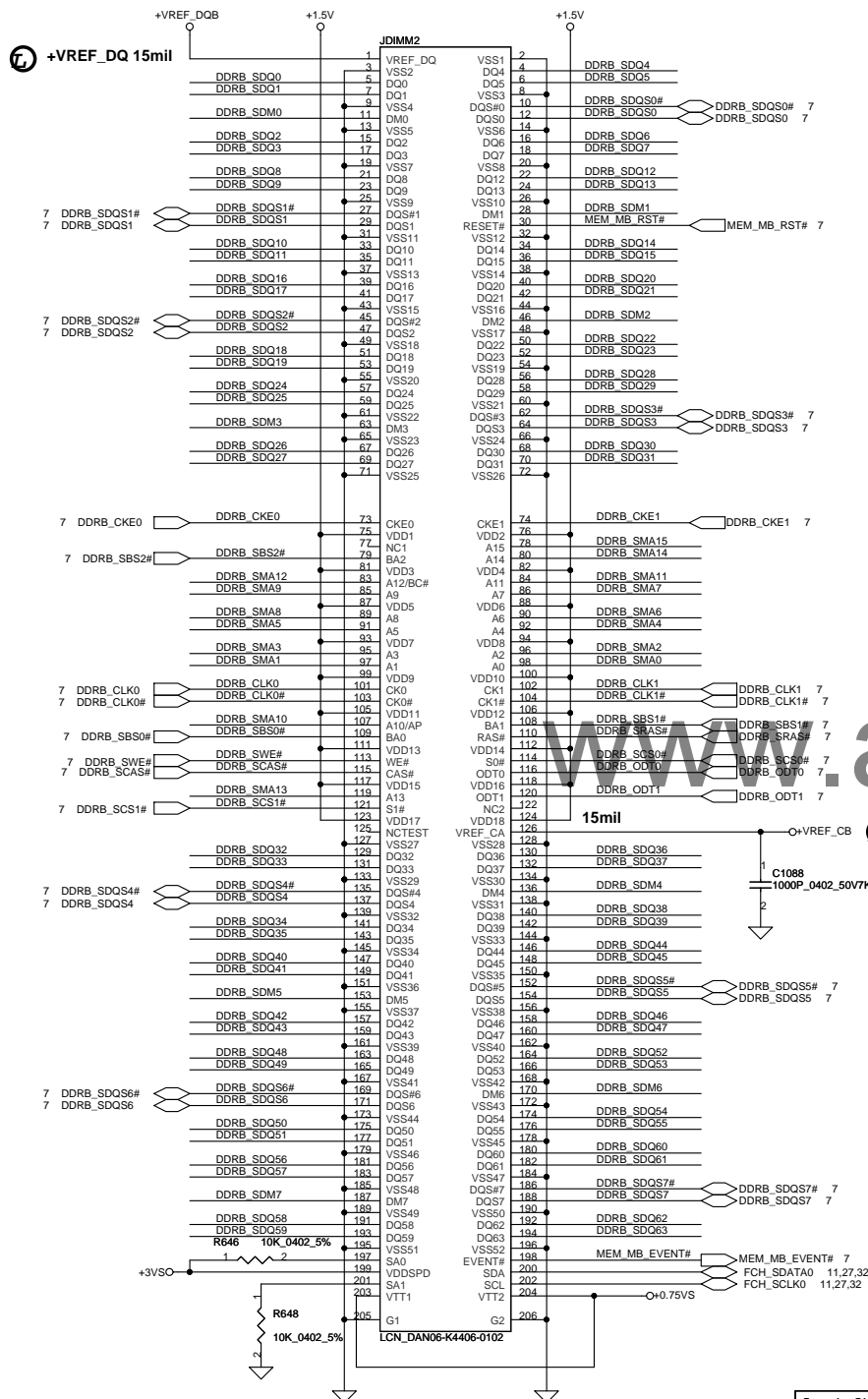
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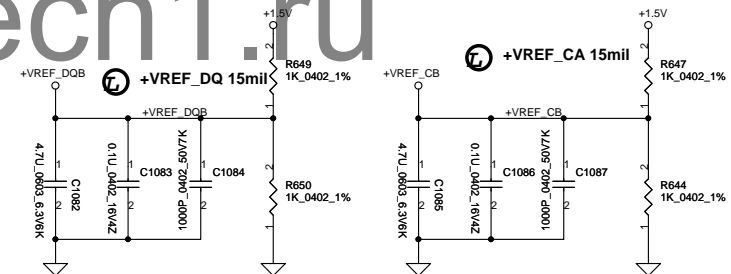
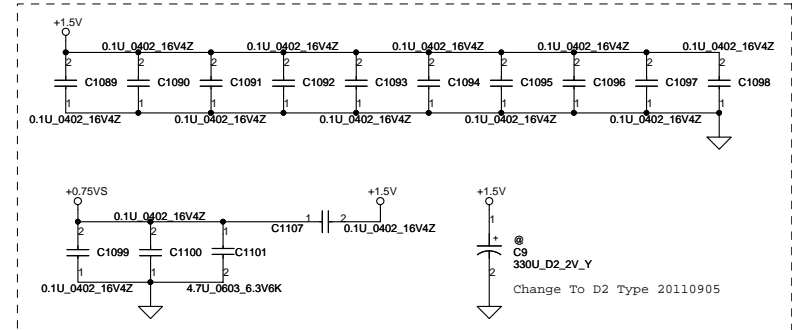
Place near DIMM1



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				Date:	Tuesday, January 10, 2012
				Sheet	11 of 54



Place near DIMM2



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				Date:	Tuesday, January 10, 2012
				Sheet	12 of 54

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				Date: Tuesday, January 10, 2012	Sheet 13 of 54	

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				Date: Tuesday, January 10, 2012	Sheet 14 of 54	

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				Date: Tuesday, January 10, 2012	Sheet 15 of 54	

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				Date: Tuesday, January 10, 2012	Sheet 16 of 54	

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				Date:	Tuesday, January 10, 2012	Sheet 17 of 54

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				Date: Tuesday, January 10, 2012	Sheet 18 of 54	

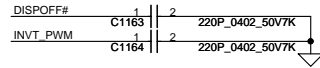
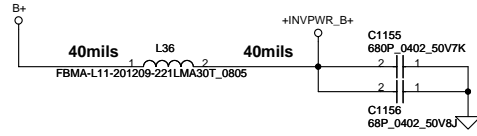
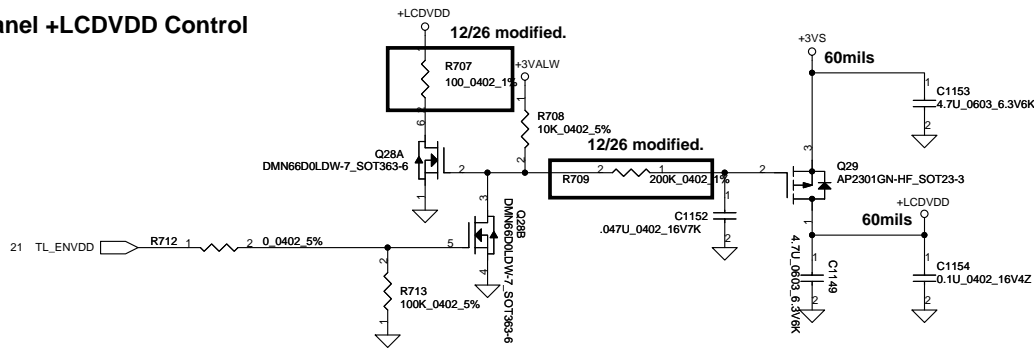
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				C	4019IF
				Date:	Rev
				Tuesday, January 10, 2012	A
				Sheet	19 of 54

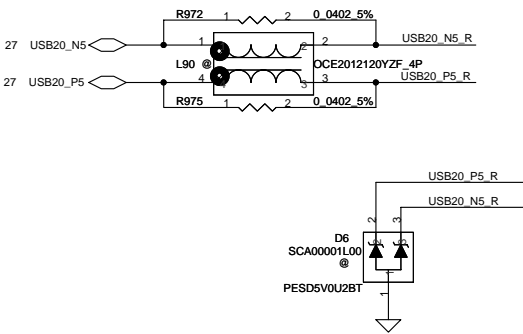
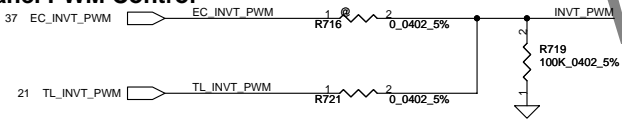
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				Date Tuesday, January 10, 2012	Sheet 20 of 54
Rev A					

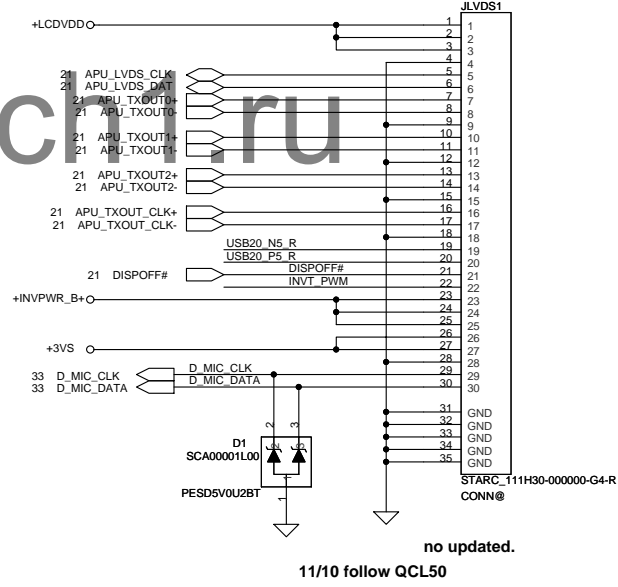
Panel +LCDVDD Control



Panel PWM Control

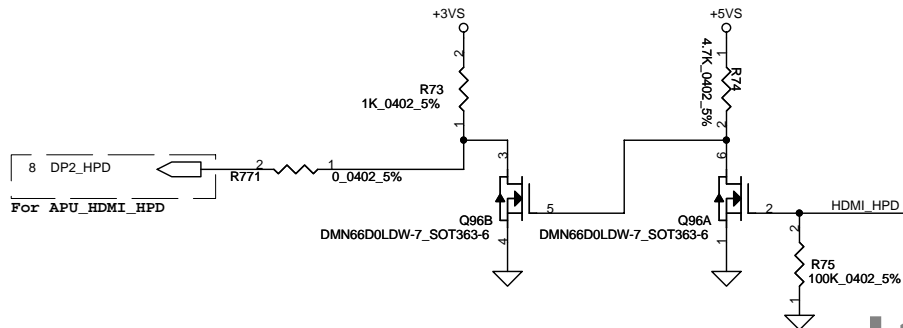
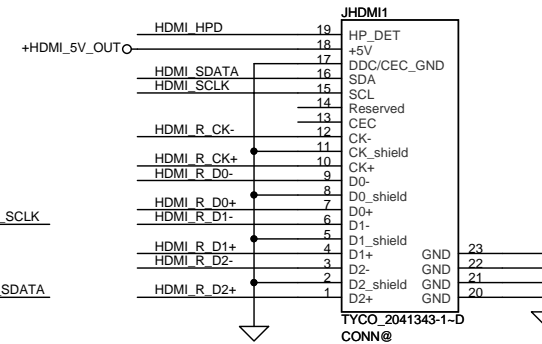
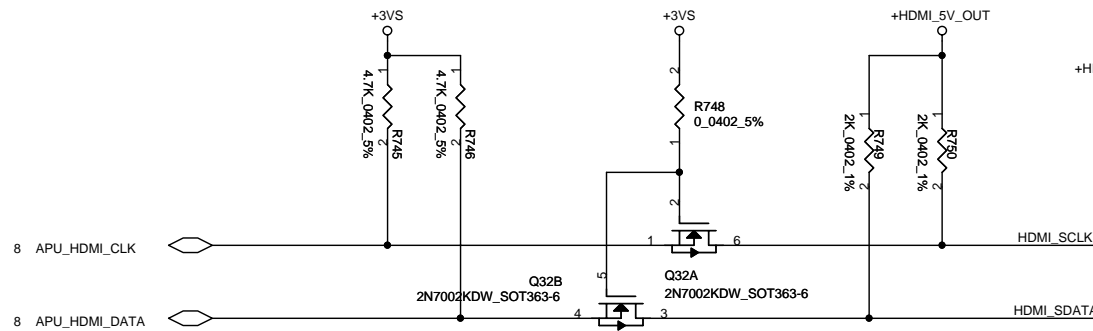


LVDS Connector

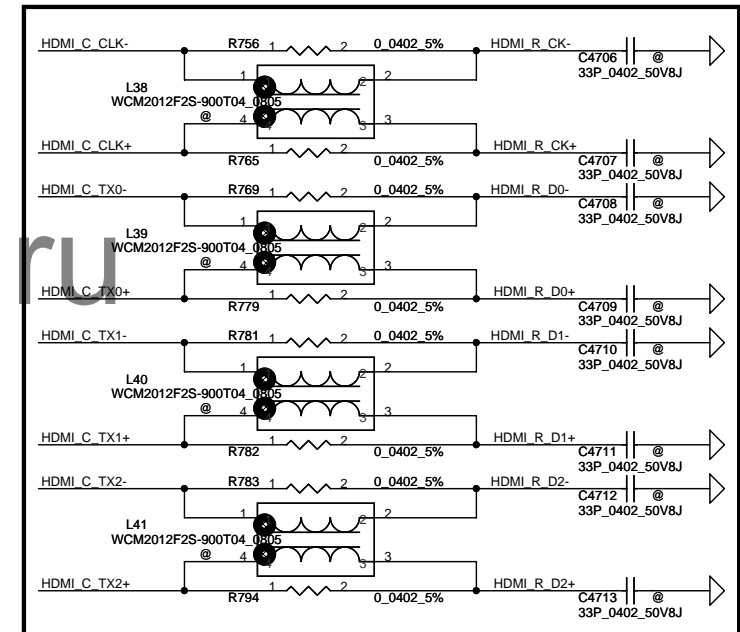


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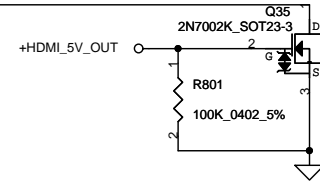
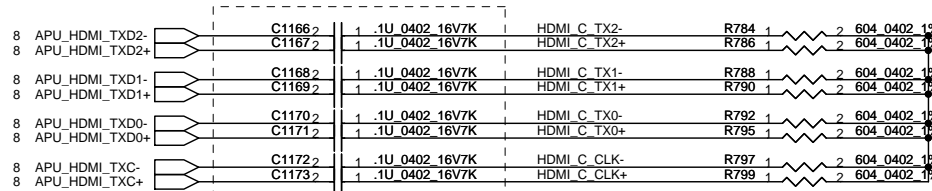
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				Date:	Tuesday, January 10, 2012
				Sheet	22 of 54



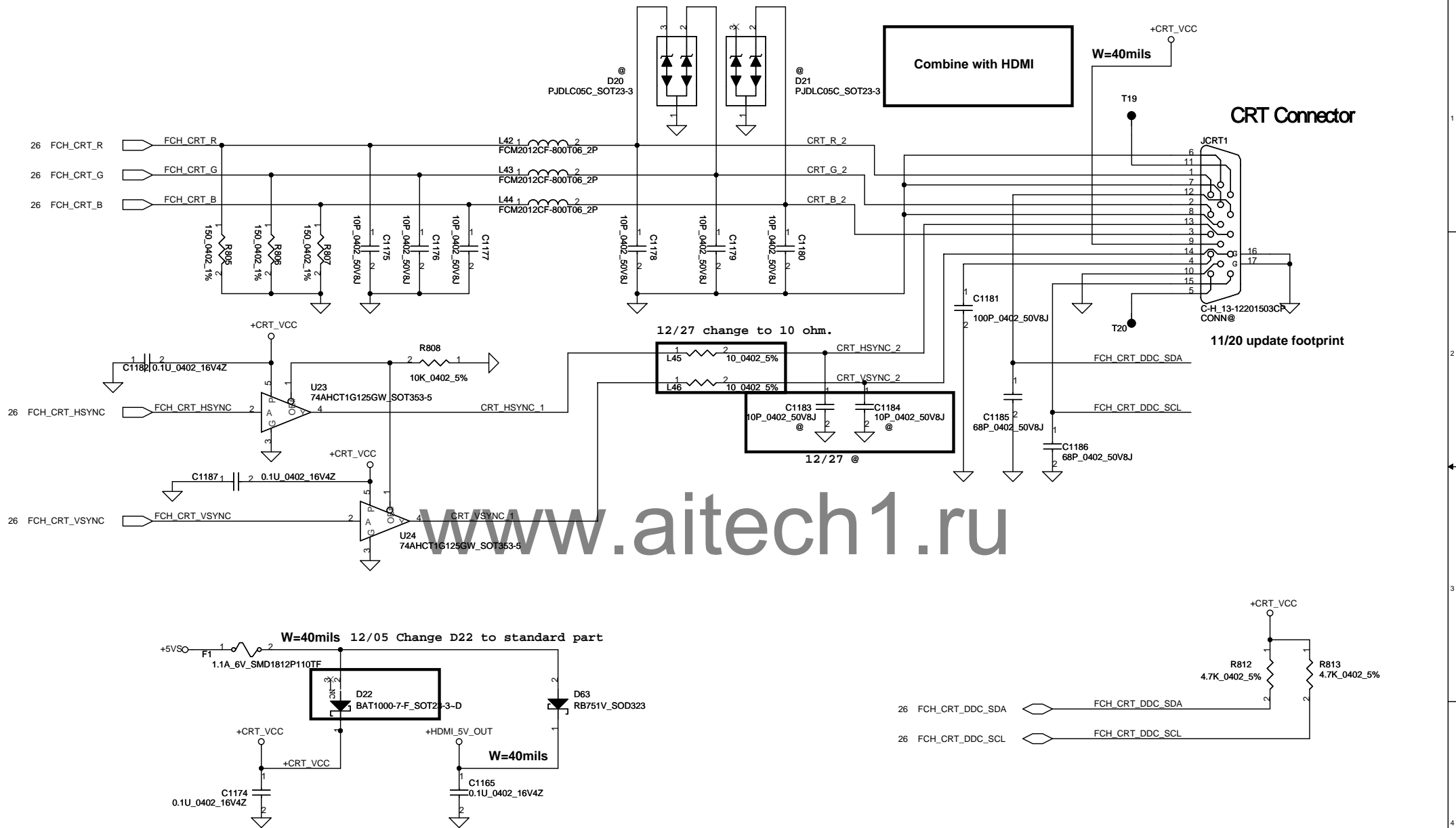
12/7 Swap signals for routing smoothly



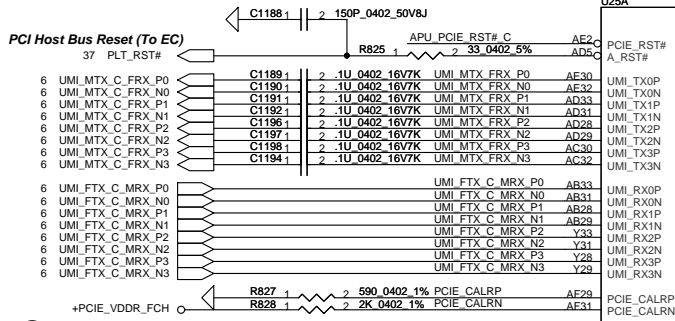
Close to HDMI conn



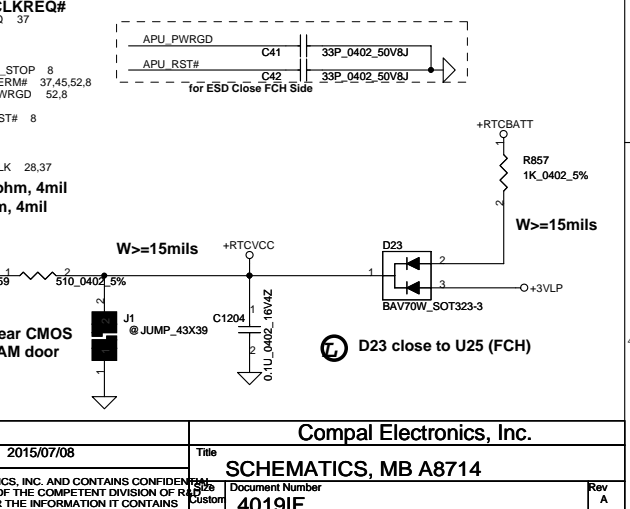
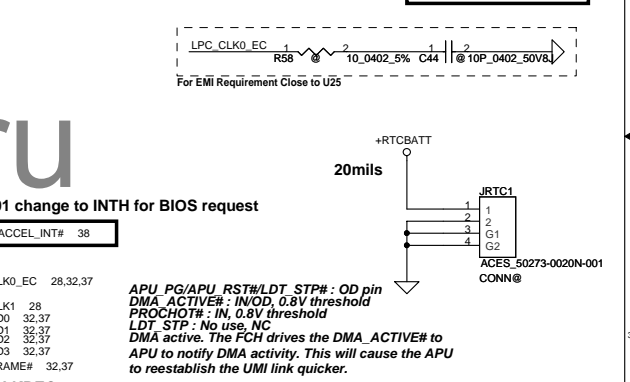
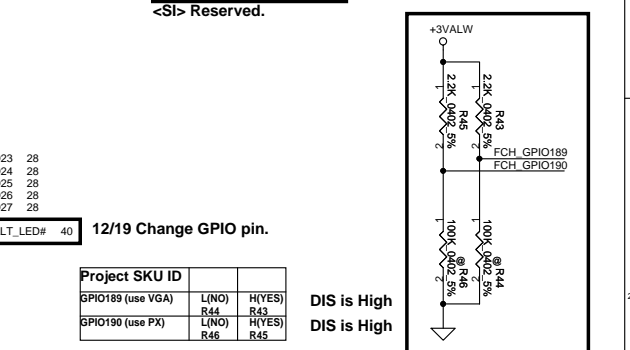
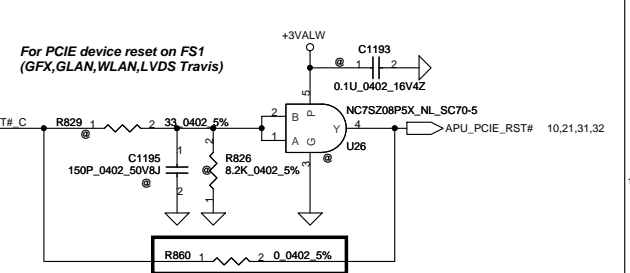
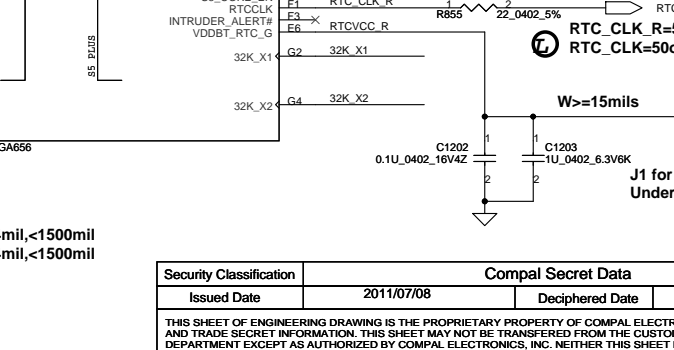
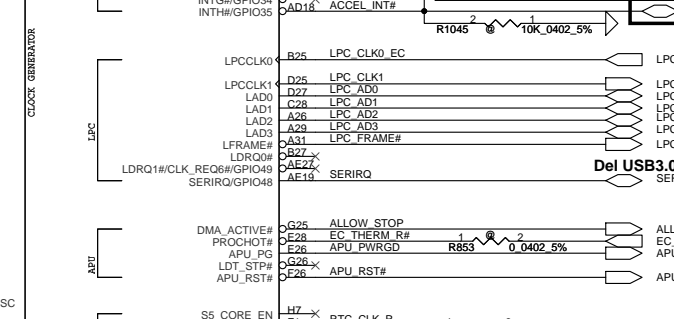
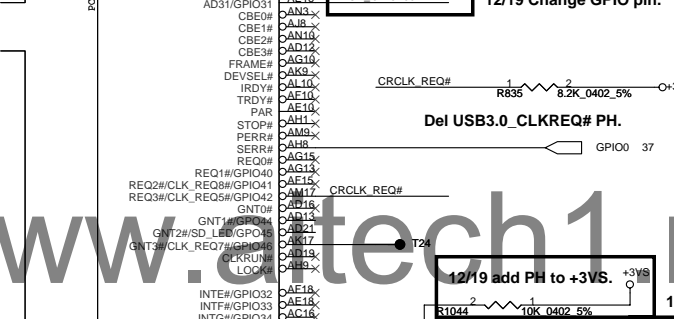
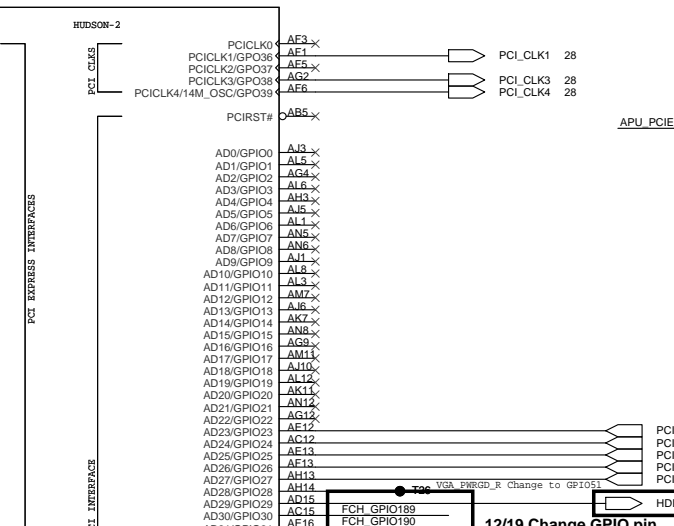
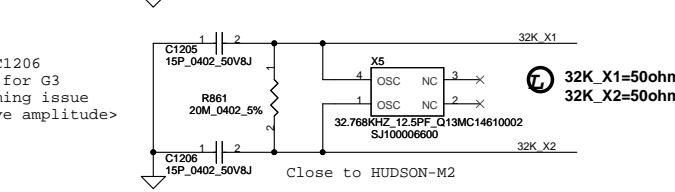
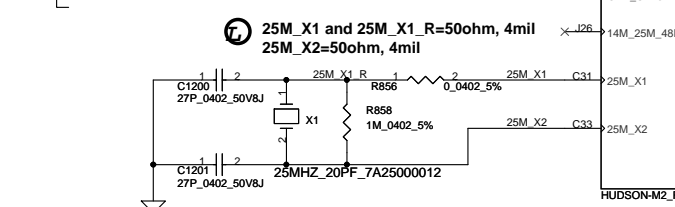
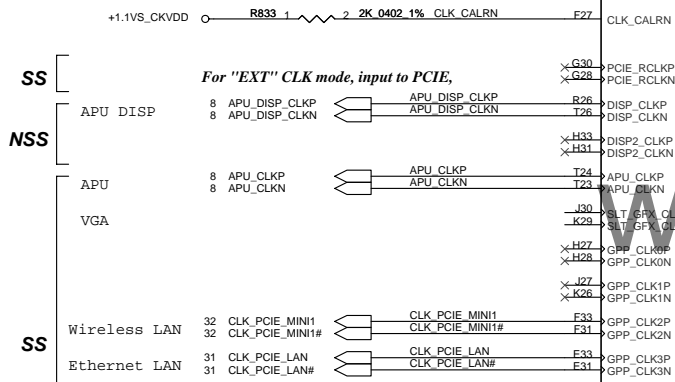
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				Date:	Tuesday, January 10, 2012
				Sheet	23 of 54



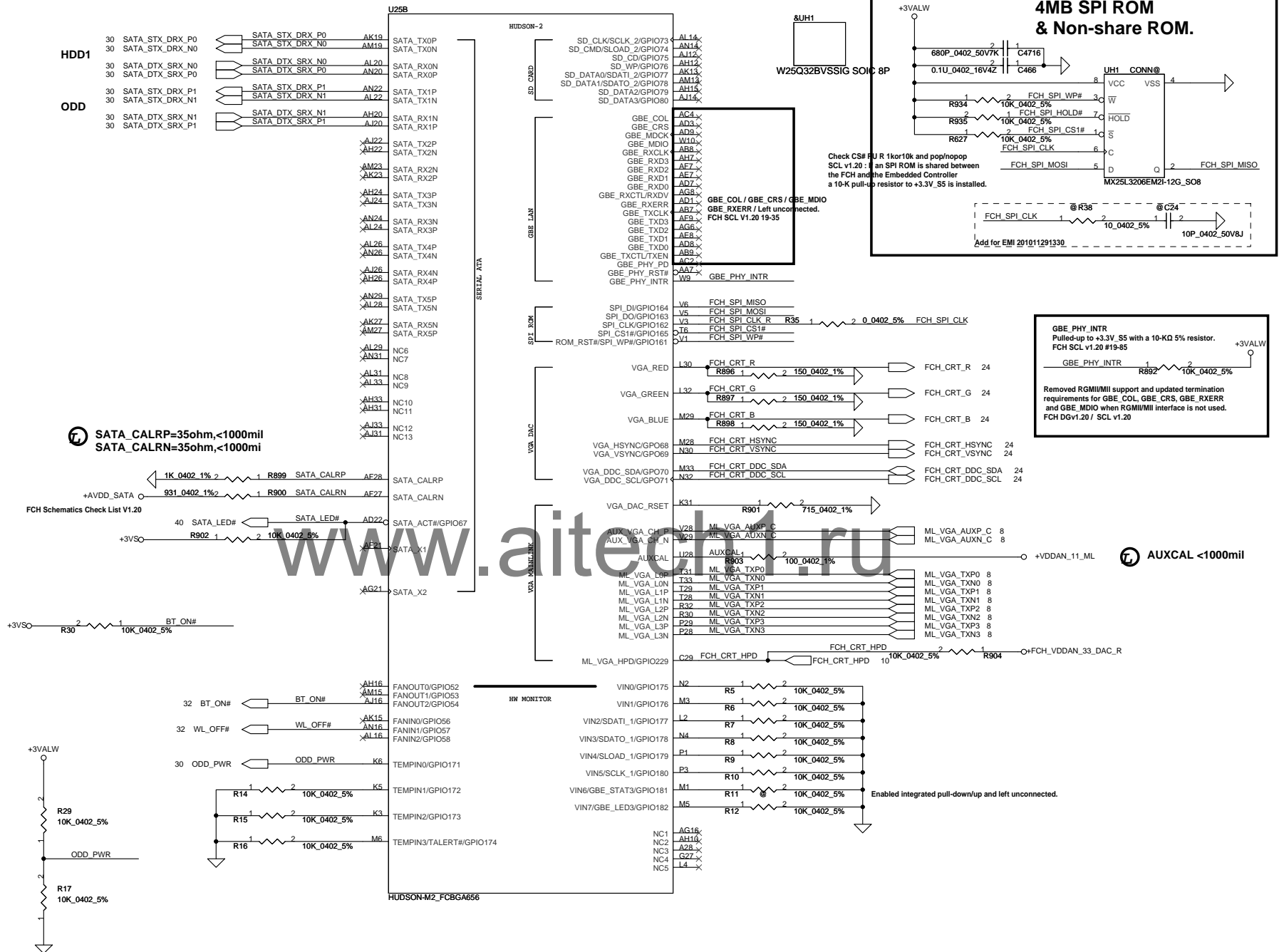
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				Date:	Tuesday, January 10, 2012
				Sheet	24 of 54



PCI CalRP R=50ohm, 4mil, <1000mil
PCI CalRN R=50ohm, 4mil, <1000mil

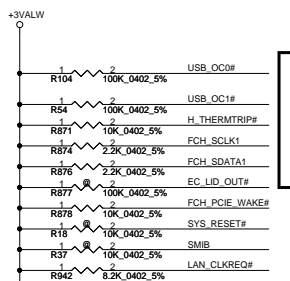


C1205, C1206
Change for G3
RTC timing issue
<improve amplitude>



ThermTrip:
Need level shift from +3VALW to +1.5V
Note: Ensure FCH internal pull-up resistor
to +3.3V S5 is disabled to prevent leakage
when APU is powered down.

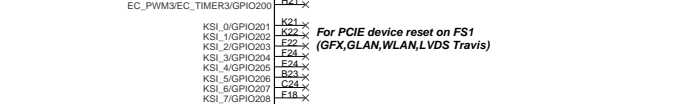
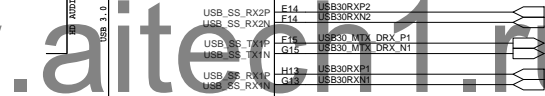
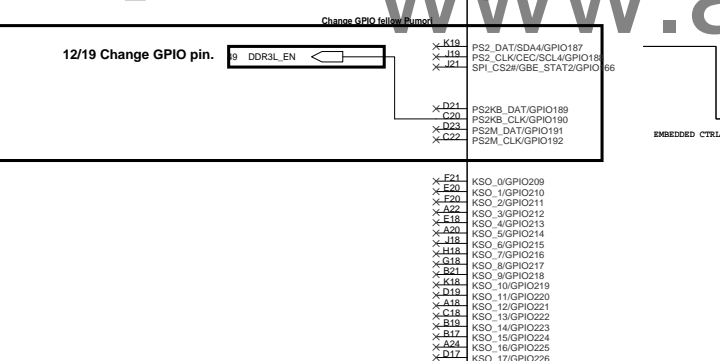
FCH GEVENT (S5 domain)
with isolation circuit to avoid leakage



1 R887 2.2K 0402_5% TEST0

1 R889 2.2K 0402_5% TEST1

1 R890 2.2K 0402_5% TEST2

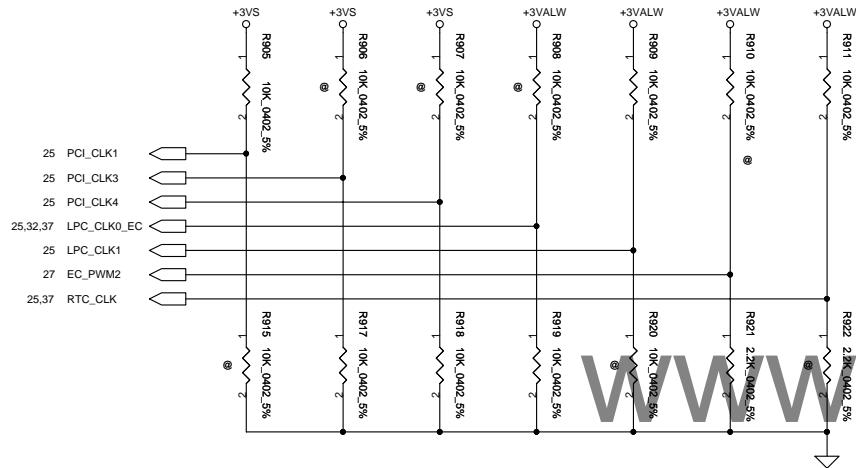


- ✗ For PCIE device reset on FS1
- ✗ (GFX, GLAN, WLAN, LVDS Travis)

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	1	2	3	4	5
	100%	100%	100%	100%	100%

STRAP PINS

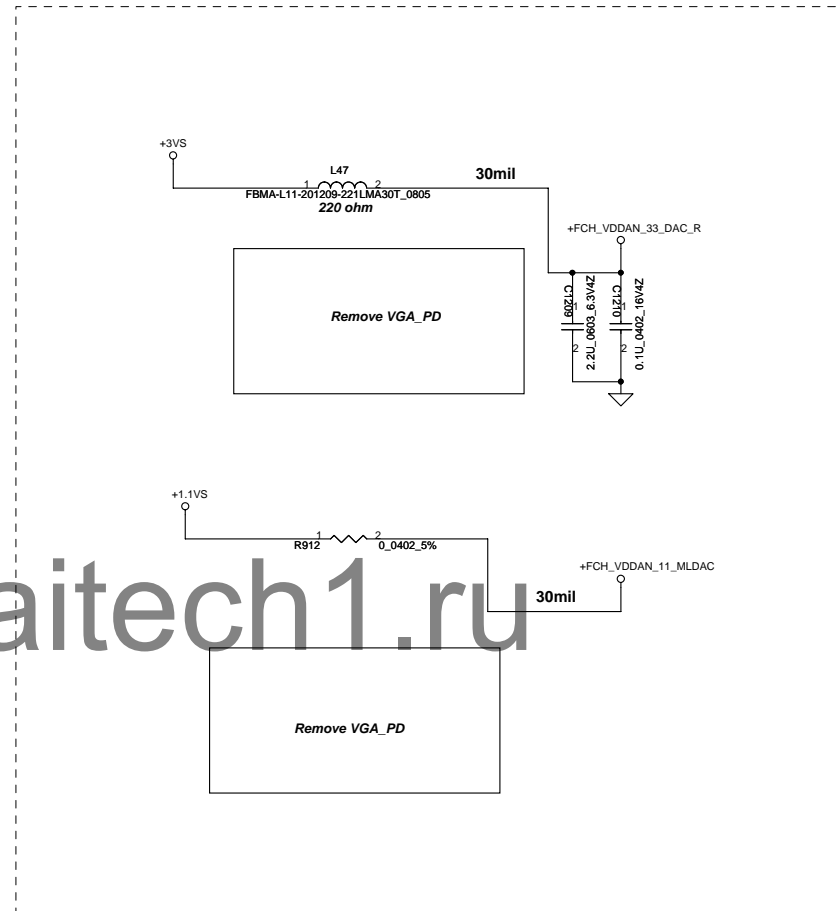
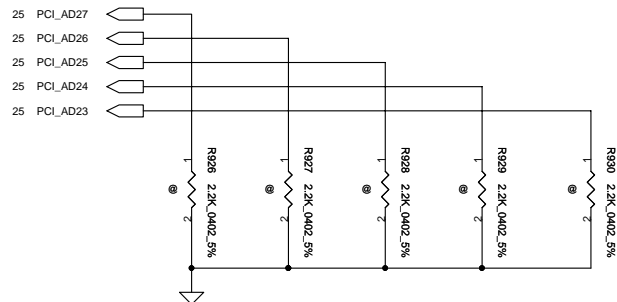
	PCI_CLK1	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	EC_PWM2	RTC_CLK
PULL HIGH	ALLOW PCIE GEN2 DEFAULT	USE DEBUG STRAPS	NON_FUSION CLOCK MODE	EC ENABLED	CLKGEN ENABLED	LPC ROM	S5 PLUS MODE DISABLED DEFAULT
PULL LOW	FORCE PCIE GEN1	IGNORE DEBUG STRAP DEFAULT	FUSION CLOCK MODE DEFAULT	EC DISABLED	CLKGEN DISABLE	SPI ROM DEFAULT	S5 PLUS MODE ENABLED



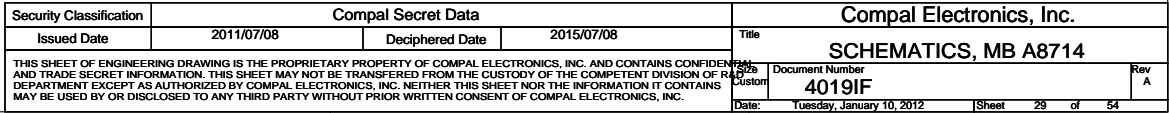
DEBUG STRAPS

FCH HAS 15K INTERNAL PU FOR PCI_AD[27:23]

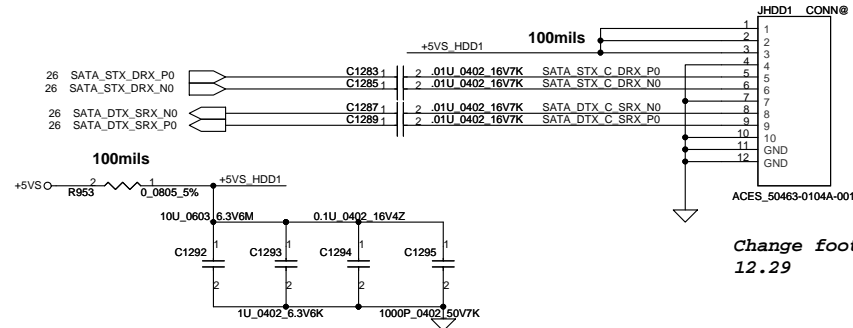
	PCI_AD27	PCI_AD25	PCI_AD24	PCI_AD23
No external R	USE PCI PLL DEFAULT	Normal REFCLK termination DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	Inverted REFCLK termination	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT



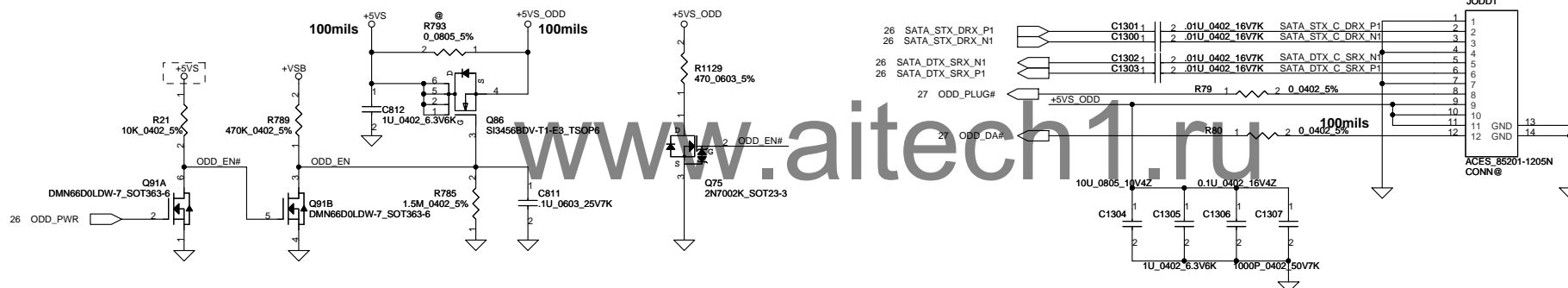
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				Date:	Tuesday, January 10, 2012
				Sheet	28 of 54



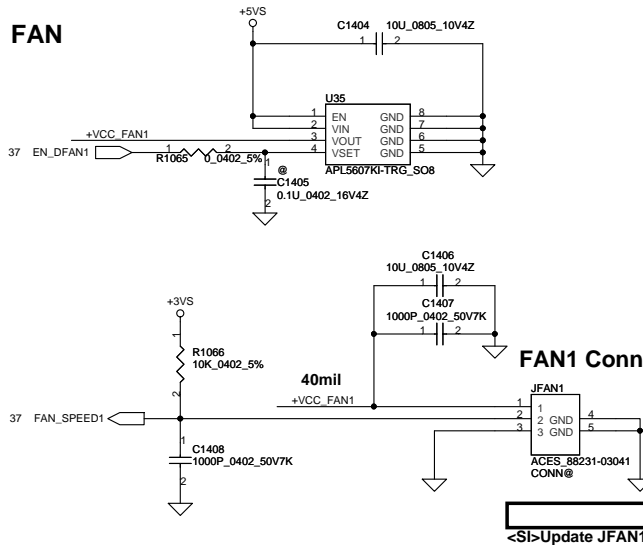
SATA HDD1 Conn.



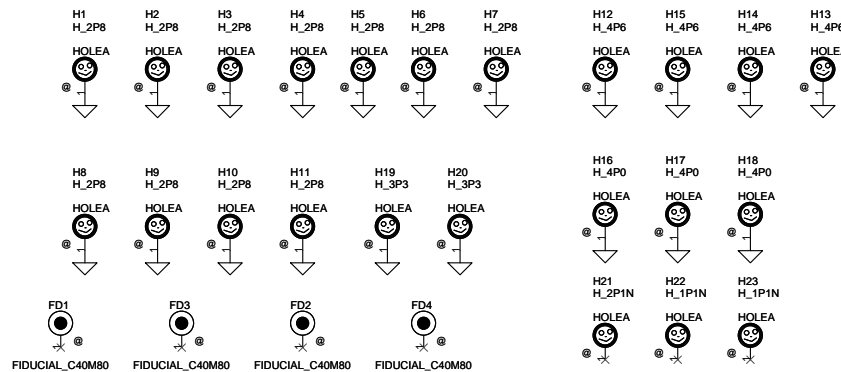
ODD conn



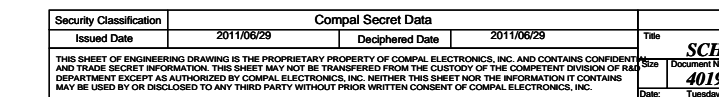
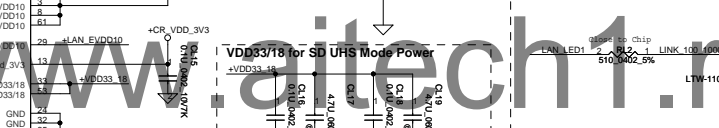
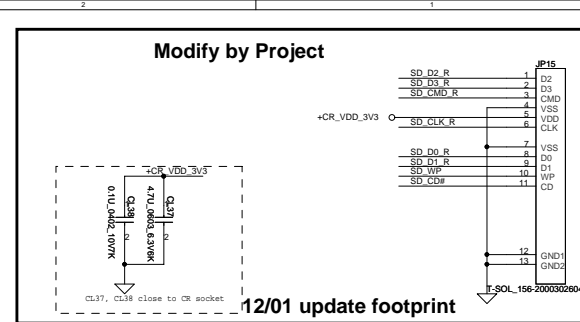
FAN



Screw Hole

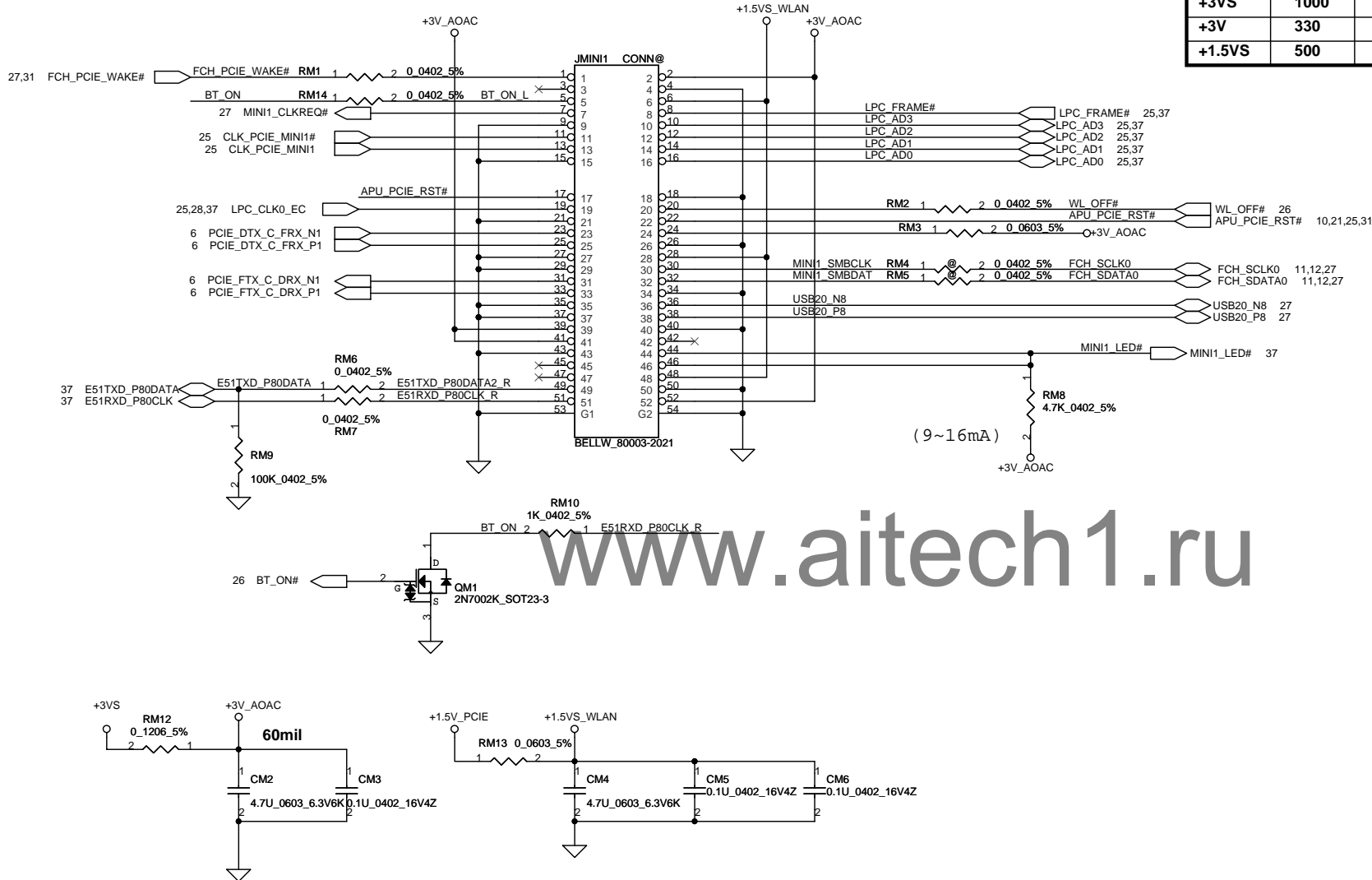


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				Date	Tuesday, January 10, 2012
				Sheet	30 of 54



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				Sheet	31 of 54

WLAN



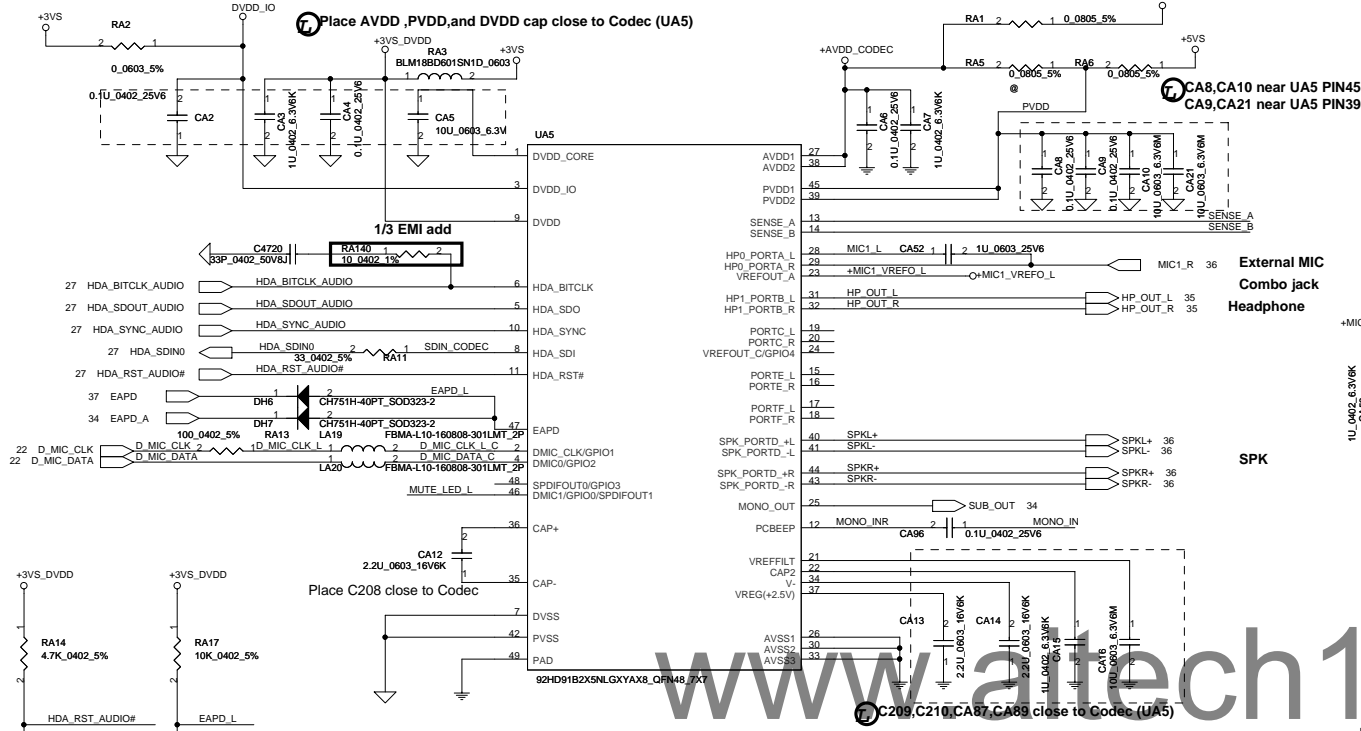
Mini Card Power Rating			
Power	Primary Power (mA)		Auxiliary Power (mA)
	Peak	Normal	Normal
+3VS	1000	750	
+3V	330	250	250 (wake enable)
+1.5VS	500	375	5 (Not wake enable)

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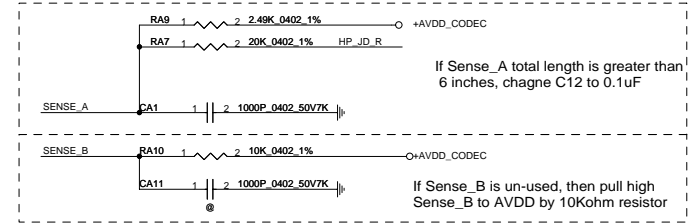
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				Date:	Tuesday, January 10, 2012
				Sheet	32 of 54

Notes:
Keep PVDD supply and speaker traces routed on the DGND plane.
Keep away from AGND and other analog signals

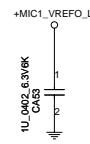
Place AVDD, PVDD, and DVDD cap close to Codec (UA5)



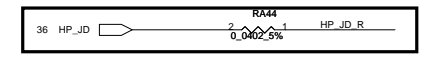
Place close to UA5 PIN 13



Place close to UA5 PIN 14



12/5 Audio jack change to normal open, so remove MOS



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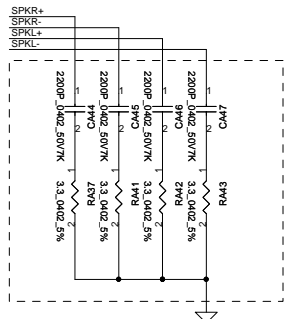
Place C208 close to Codec

C209, C210, CA87, CA89 close to Codec (UA5)

Need confirmed.

12/7 Change to single package

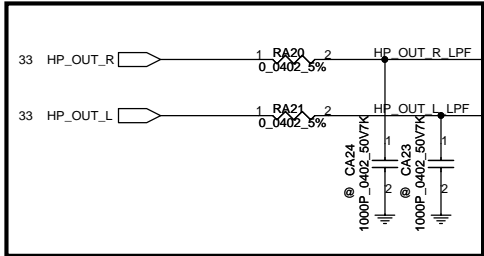
Close to Audio Codec (UA5)



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Customer				Document Number	LA-8551P
Date:				Tuesday, January 10, 2012	Sheet 33 of 54

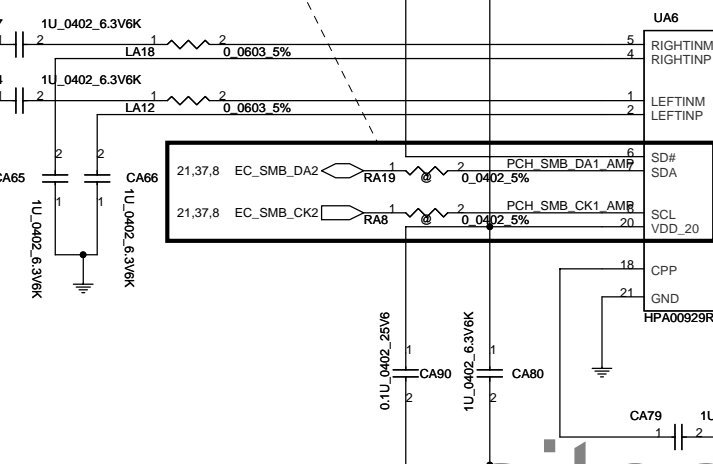
Headphone amplifier

12/05 Add LPF for HP requirement

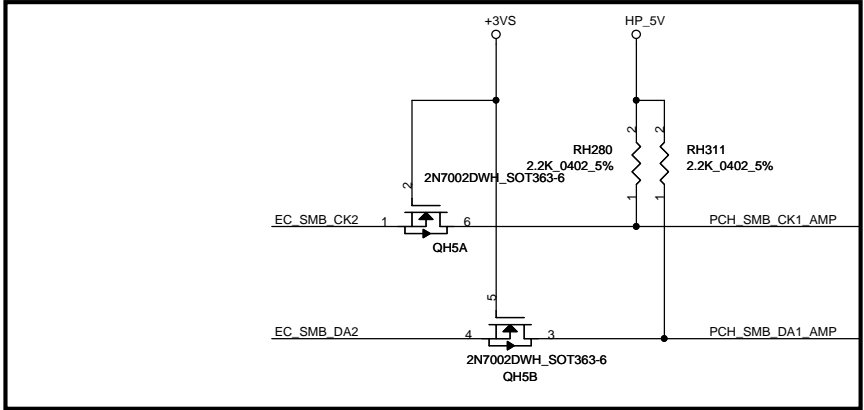


<SI> BOM update :RA20,RA21 4.7K-->0
CA24,CA23 SMT-->@

12/05 Connect HP AMP SMBus to EC

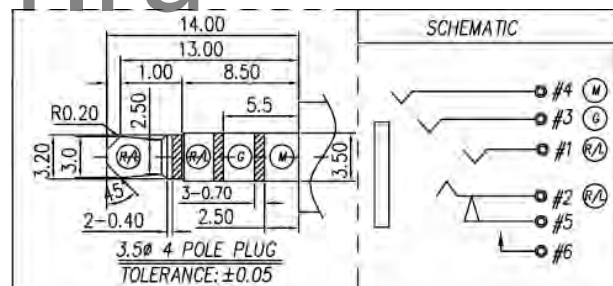
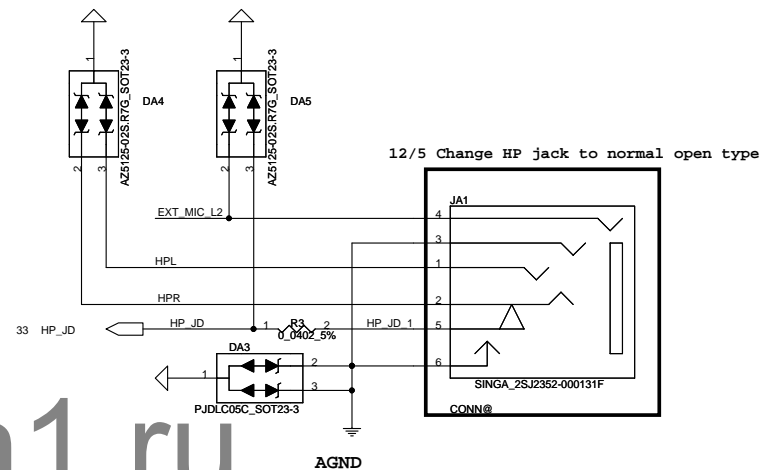
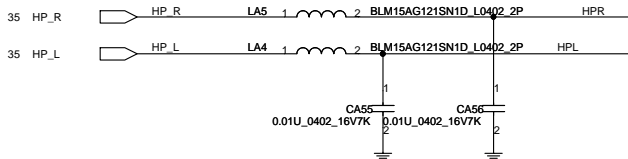
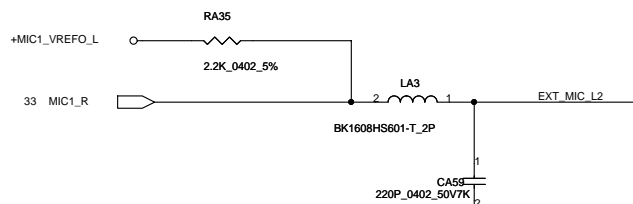
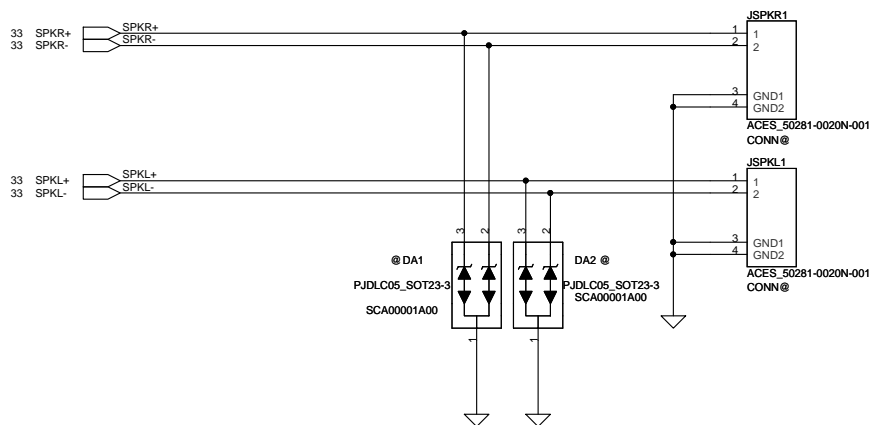


12/05 Reserve leavel shift Connect to EC

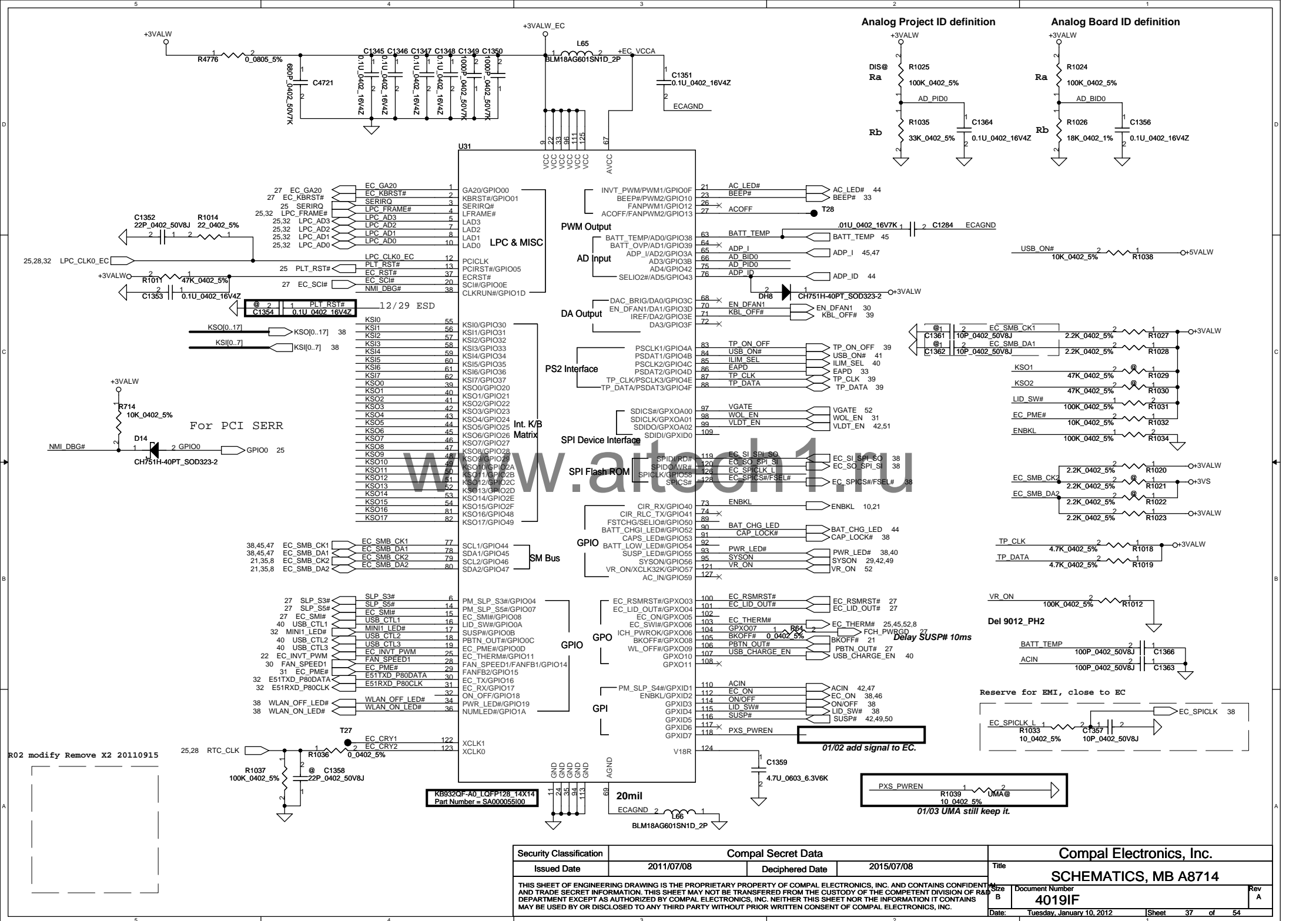


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					Date:	Tuesday, January 10, 2012	Sheet	35 of 54

SPK conn



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				Custom	40191F	A
				Date:	Tuesday, January 10, 2012	Sheet 36 of 54



Power

37,46 EC_ON \rightarrow EC_ON

ON/OFFBTN#

ON/OFF 37

51ON# 44

+3V/ALW

R1040
100K_0402_5%

D26
BAV70W_SOT323-3

C1365
1000P_0402_50V7K

Q44
2N7002K_SOT23-3

R1043
10K_0402_5%

The schematic diagram illustrates the HP3DC2 module's internal components and their connections. The central component is the U60 IC, which is connected to a +3VALW supply. The IC's pins are configured as follows:

- Vdd_IO** (Pin 1) is connected to +3VALW.
- SCL/SPC** (Pin 4) is connected to EC SMB CK1 (37.45, 47).
- SDA/SDI/SDO** (Pin 5) is connected to EC SMB DA1 (37.45, 47).
- SDO/SA0** (Pin 7) is connected to +3VALW.
- CS** (Pin 8) is connected to +3VALW.
- NC** (Pin 2) is connected to +3VALW.
- NC** (Pin 3) is connected to +3VALW.
- INT2** (Pin 9) is connected to +3VALW.
- INT1** (Pin 11) is connected to +3VALW.
- VDD** (Pin 14) is connected to +3VALW.
- GND** (Pin 12) is connected to GND.
- RES** (Pin 13) is connected to GND.
- RES** (Pin 15) is connected to GND.
- RES** (Pin 16) is connected to GND.

The IC is connected to a network of resistors and capacitors:

- R167** (10K_0402_5%) is connected between +3VALW and the IC's Vdd_IO pin.
- R168** (0_0402_5%) is connected between the IC's Vdd_IO pin and GND.
- C218** (0.1U_0402_16V7K) is connected between the IC's Vdd_IO pin and GND.
- C219** (10U_0603_6.3V6M) is connected between the IC's Vdd_IO pin and GND.

The module also includes two LEDs:

- WLAN_ON_LED#** (Pin 5) is connected to +3VALW.
- WLAN_OFF_LED#** (Pin 2) is connected to +3VALW.

The module is labeled with the part number **HP3DC2**.

[illegible][illegible]

CONN@

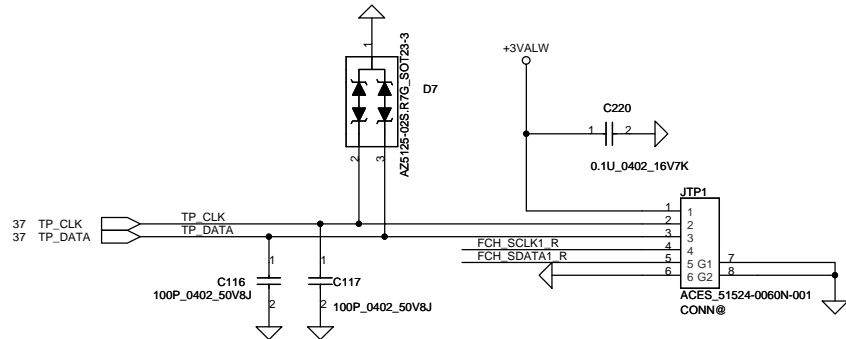
Conn footprint
Down contact

KSO15	C1380	2	100P_0402_50V8J
KSO14	C1383	2	100P_0402_50V8J
KSO13	C1384	2	100P_0402_50V8J
KSO12	C1386	2	100P_0402_50V8J
KSI0	C1388	2	100P_0402_50V8J
KSO11	C1390	2	100P_0402_50V8J
KSO10	C1392	2	100P_0402_50V8J
KSI1	C1394	2	100P_0402_50V8J
KSI2	C1396	2	100P_0402_50V8J
KSO9	C1398	2	100P_0402_50V8J
KSI3	C1400	2	100P_0402_50V8J
KSO8	C1402	2	100P_0402_50V8J
KSO3	C1389	2	100P_0402_50V8J
KSI4	C1391	2	100P_0402_50V8J
KSO2	C1393	2	100P_0402_50V8J
KSO1	C1395	2	100P_0402_50V8J

KSO16	C1378	2	100P_0402_50V8J
KSO17	C1379	2	100P_0402_50V8J
KSO6	C1381	2	100P_0402_50V8J
KSO7	C1382	2	100P_0402_50V8J
KSO5	C1385	2	100P_0402_50V8J
KSO4	C1387	2	100P_0402_50V8J
KSQ0	C1397	2	100P_0402_50V8J
KSJ5	C1399	2	100P_0402_50V8J
KSJ6	C1401	2	100P_0402_50V8J
KSJ7	C1403	2	100P_0402_50V8J

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				Document Number	A
				4019IF	
Date	Tuesday, January 10, 2012	Sheet	38	of	54

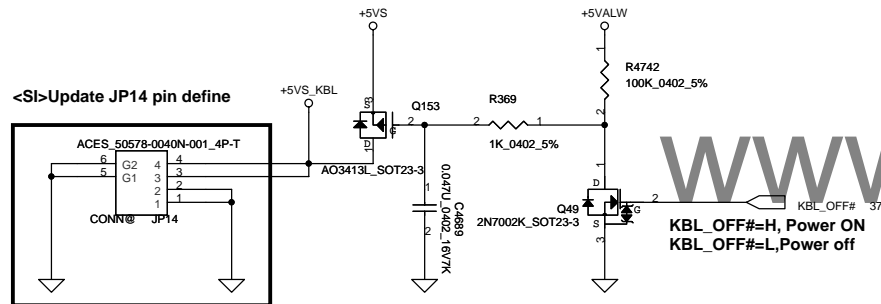
TP Conn



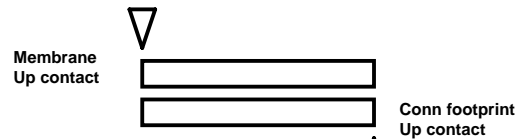
27 FCH_SCLK1 R190 0.0402_5% FCH_SCLK1_R
27 FCH_SDAT1 R210 0.0402_5% FCH_SDAT1_R

For multi-touch function

Keyboard backlight Conn



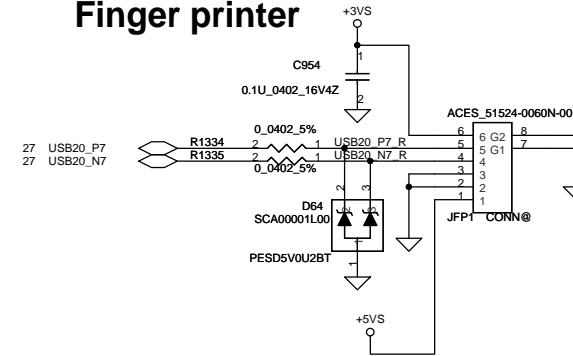
12/06 Change keyboard back light conn



The JP14 pin define must opposite

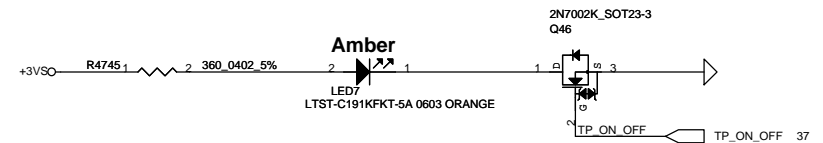
Finger printer

12/06 Change FPR pin define



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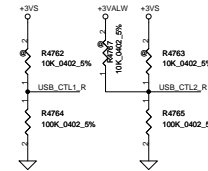
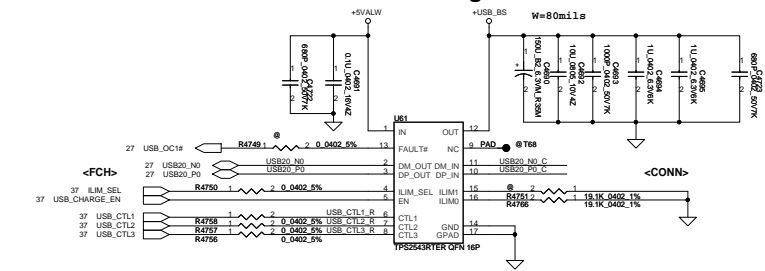
T/P On/Off LED



EC pin

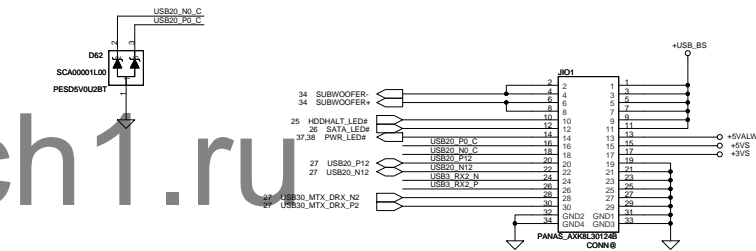
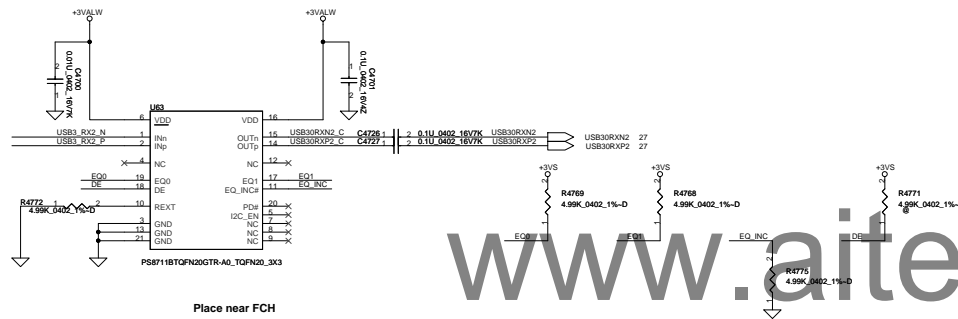
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				40191F
				Rev A
				Date: Tuesday, January 10, 2012
				Sheet 39 of 54

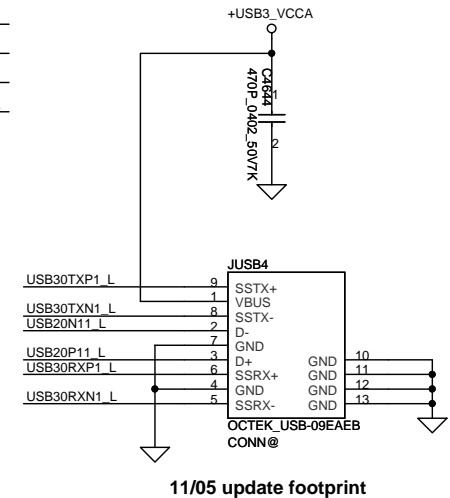
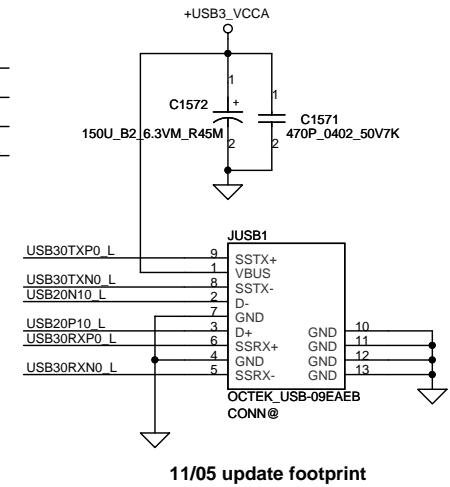
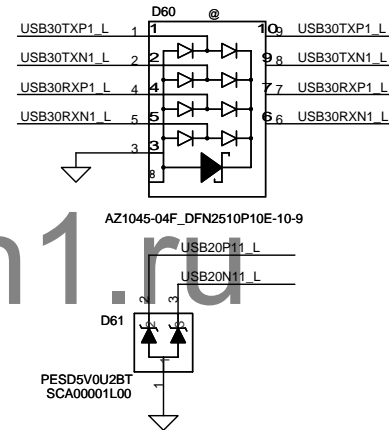
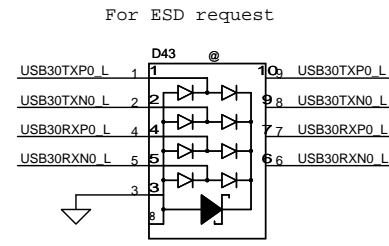
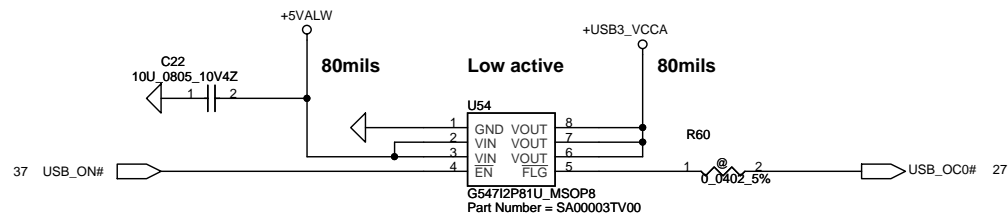
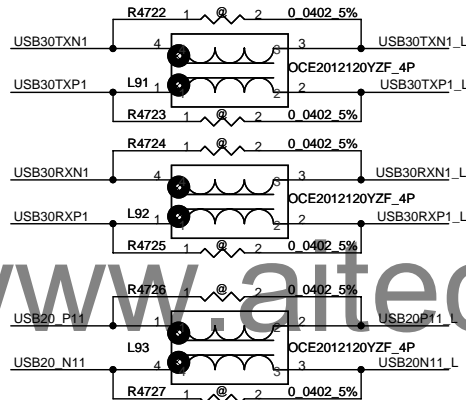
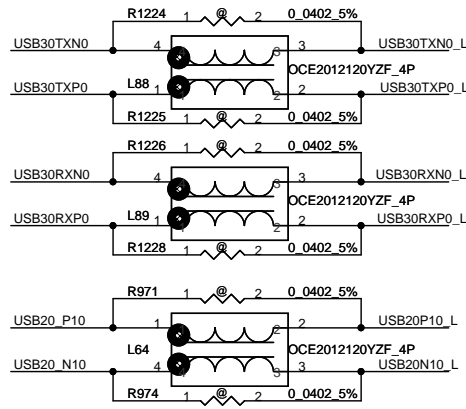
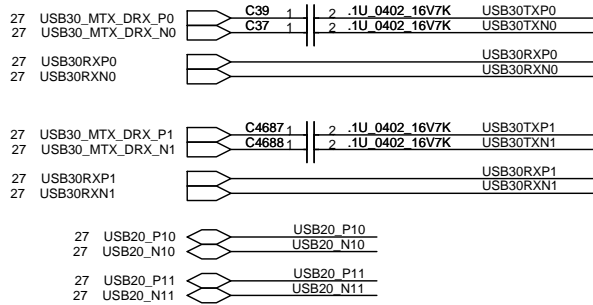
USB Charger



State	S0	S3, S4, S5
Mode	CDP	DCP
Control pin	CTL1 CTL2 CTL3 ILM_SEL	CTL1 CTL2 CTL3 ILM_SEL
	1 1 1 1	0 0 1 1

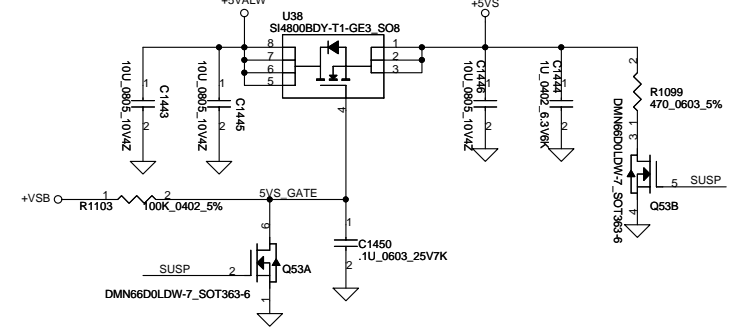
USB3.0 Repeater



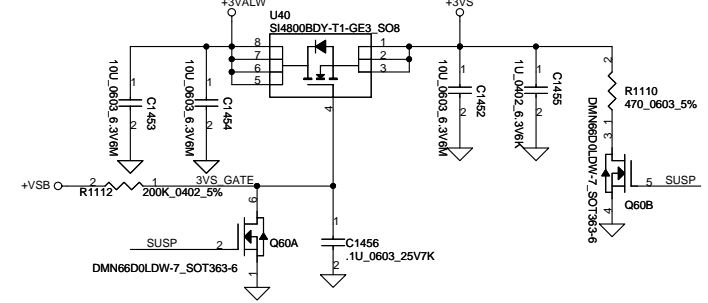


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				Date	Tuesday, January 10, 2012
				Sheet	41 of 54

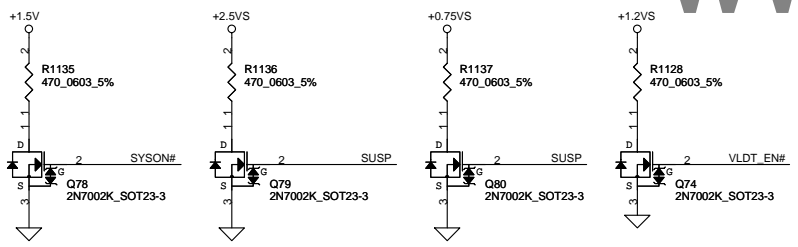
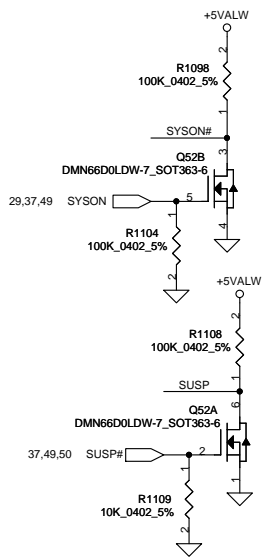
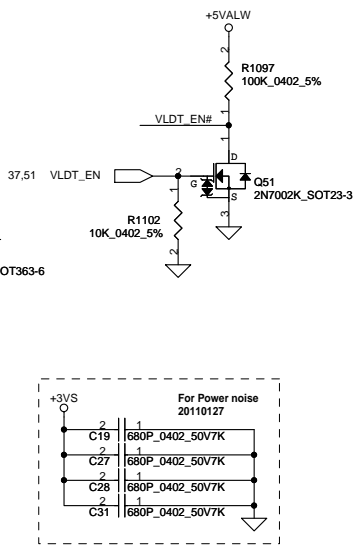
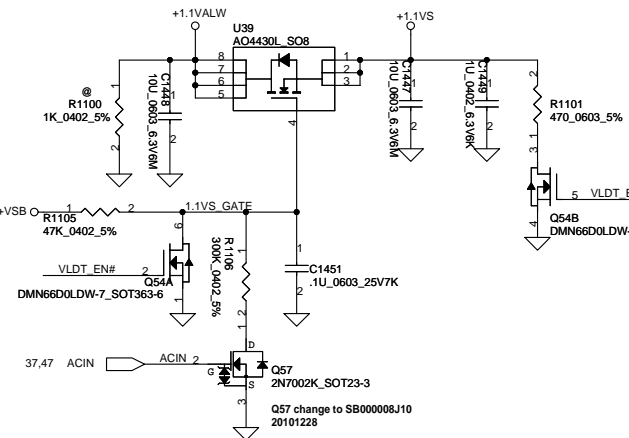
+5VALW TO +5VS (5A)



+3VALW TO +3VS (3.3A)

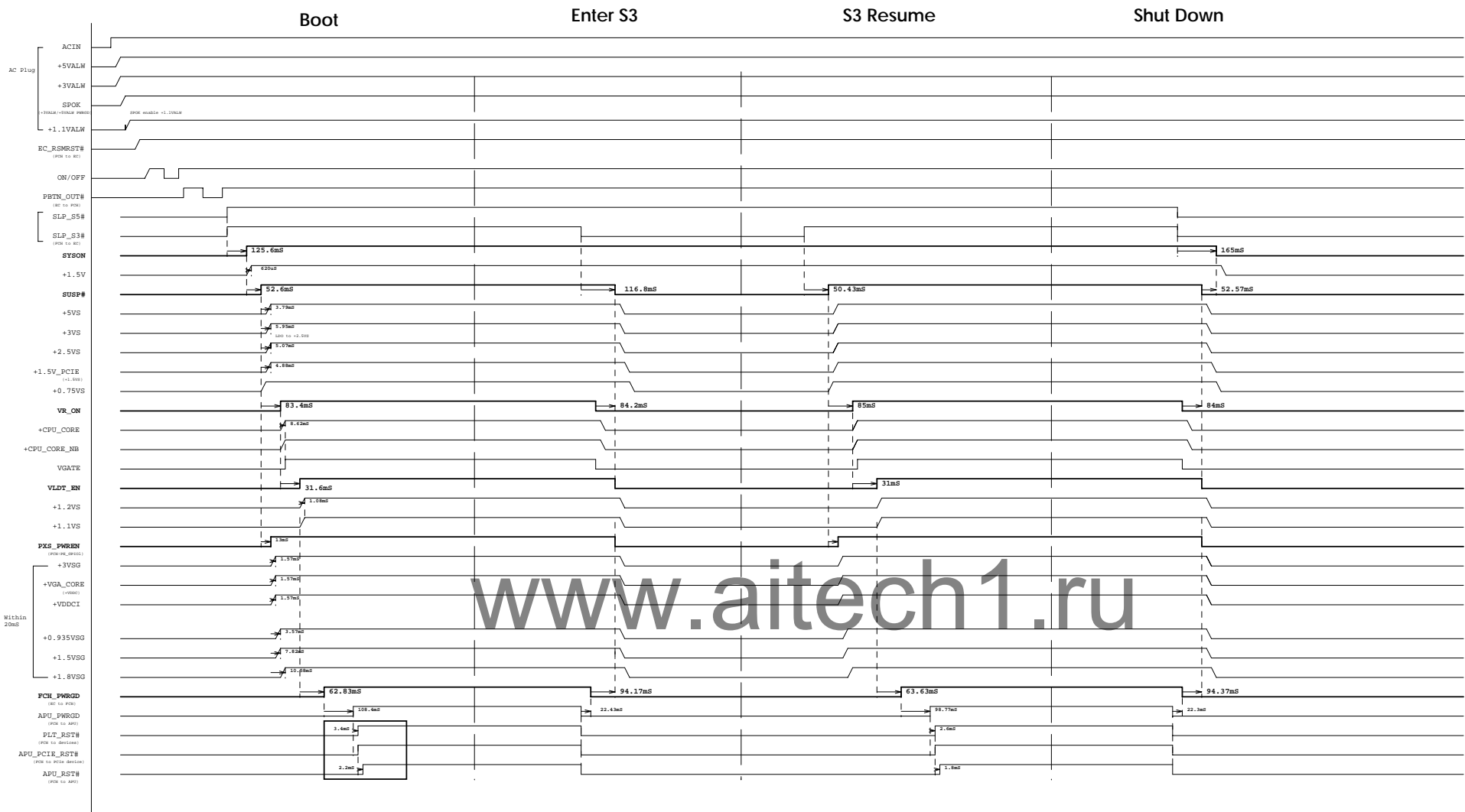


+1.1VALW TO +1.1VS (1.1A)

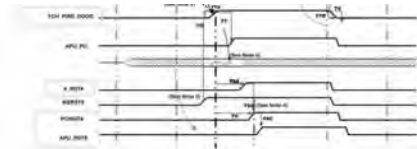


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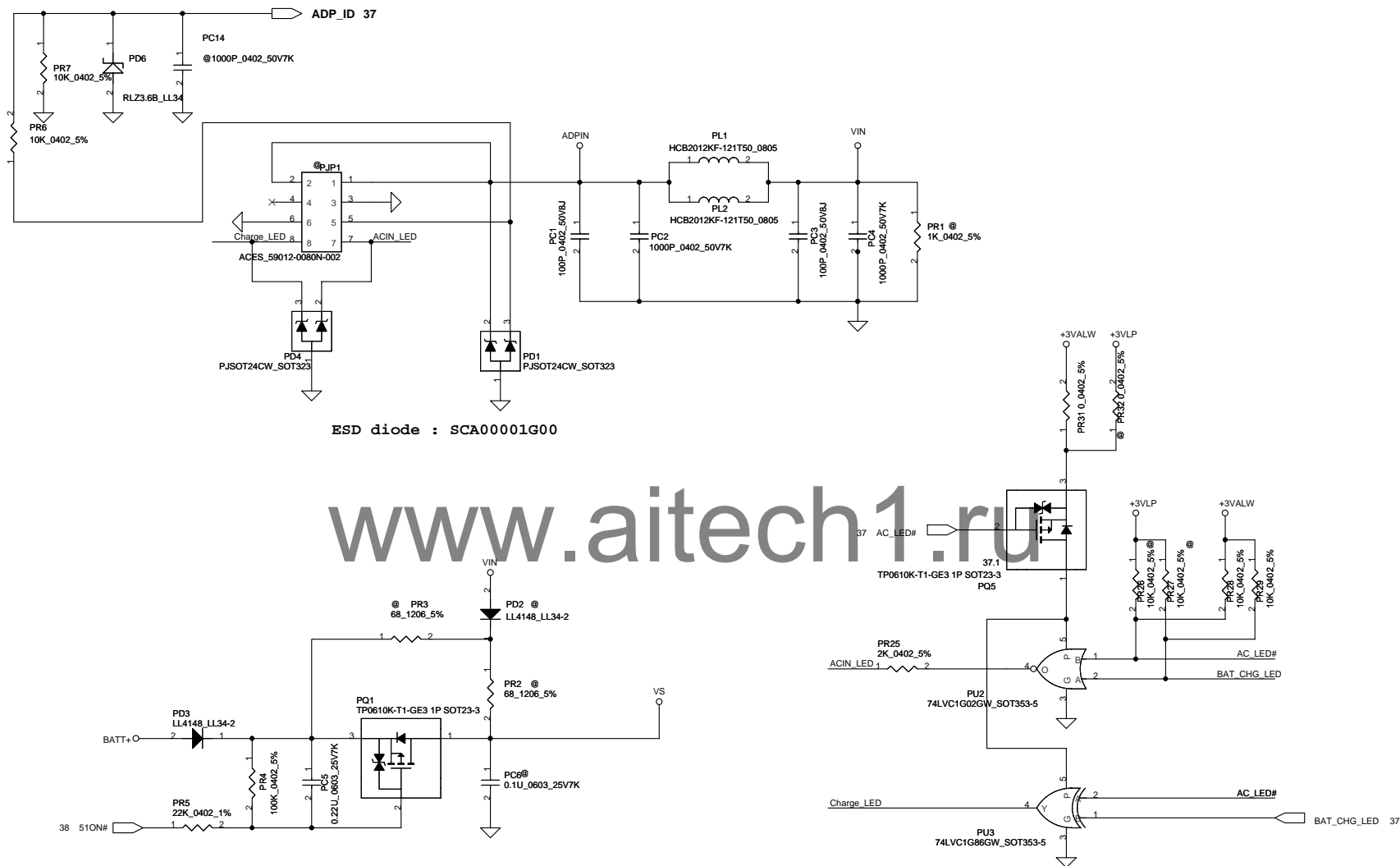
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Size	Custom	Document Number	4019IF	Rev A
Date:	Tuesday, January 10, 2012	Sheet	42	of 54



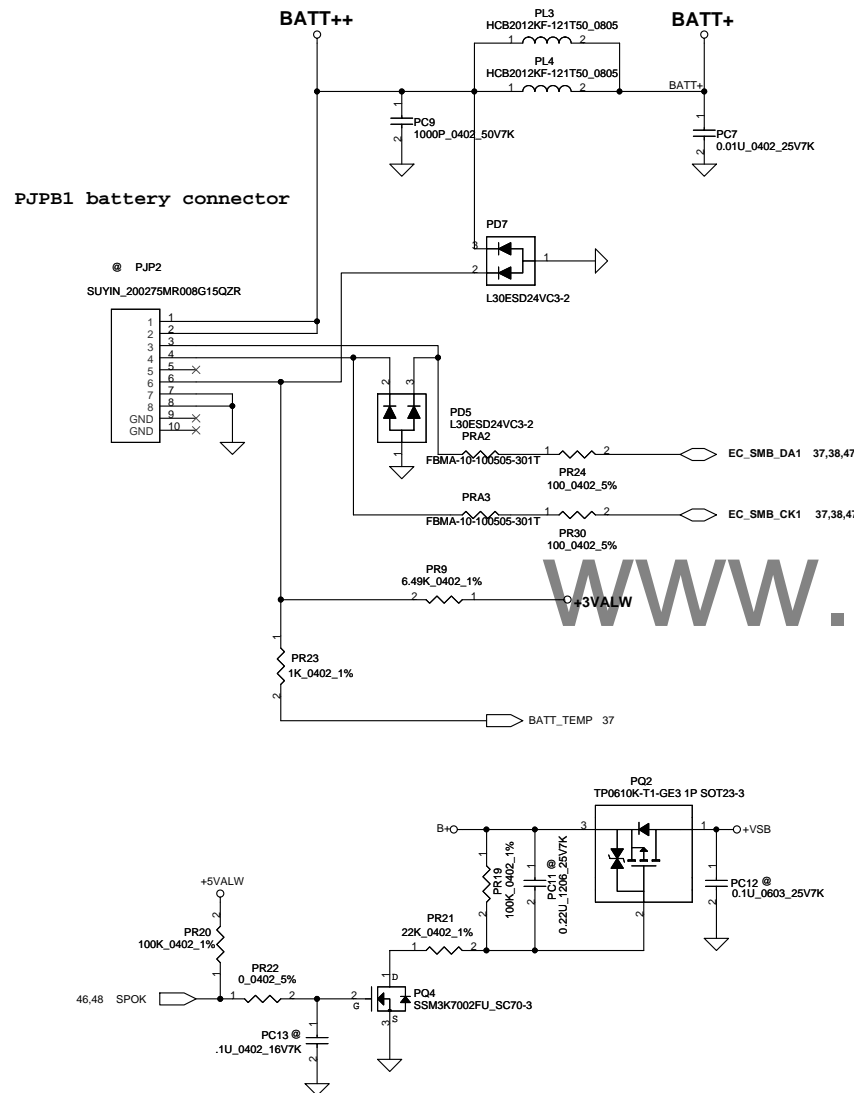
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Doc No.	40191F	Rev.	1	Page	40191F



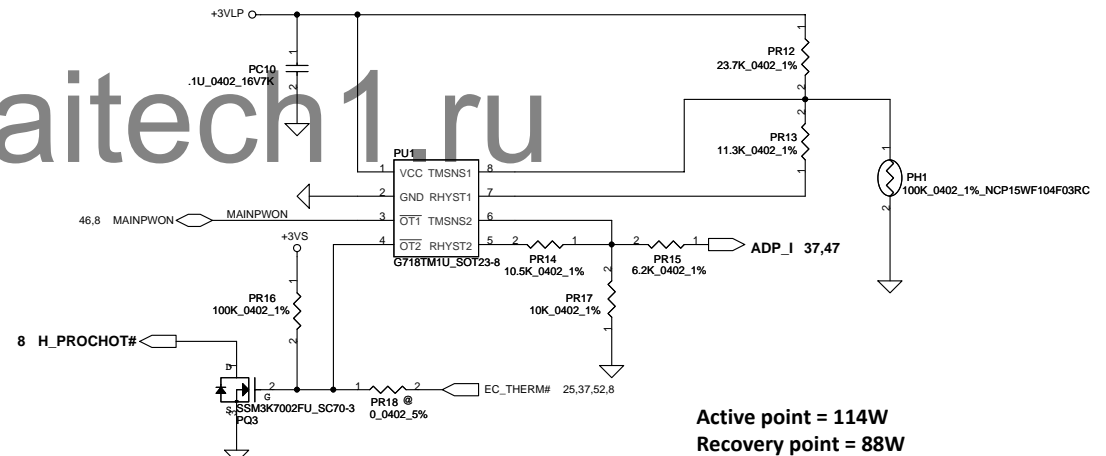
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				Date	Tuesday, January 10, 2012
				Sheet	44 of 54
				Rev	A



For KB930 --> Keep PU1 circuit
(Vth = 0.825V)

PH1 under CPU bottom side :
CPU thermal protection at 90 +/-3 degree C
Recovery at 56 +/-3 degree C

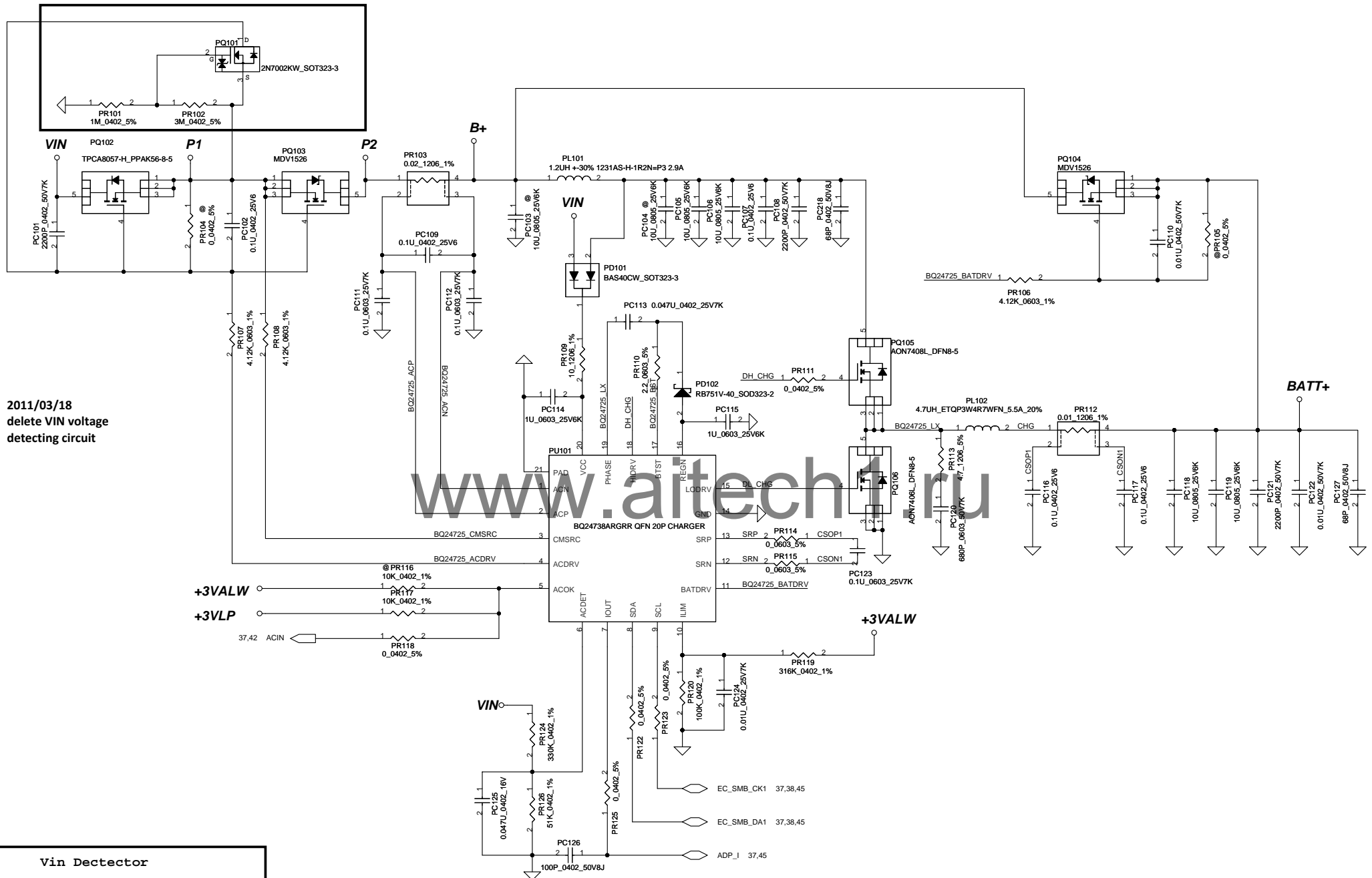
$R_{set} = 3 * R_{tmh}$
 $R_{hyst} = (R_{set} * R_{tml}) / (3 * R_{tml} - R_{set})$
 $R_{tmh} \text{ at } 90C = 7.8K, R_{tml} \text{ at } 56C = 26.1K$
 $R_{set} = 3 * 7.8K = 23.4K \Rightarrow 23.7K$
 $R_{hyst} = (23.4K * 26.1K) / (3 * 26.1K - 23.4K) = 11.12K \Rightarrow 11.3K$



Active point = 114W
Recovery point = 88W

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				Date	Tuesday, January 10, 2012
				Sheet	45 of 54
				Rev	A

for reverse input protection



2011/03/18
delete VIN voltage
detecting circuit

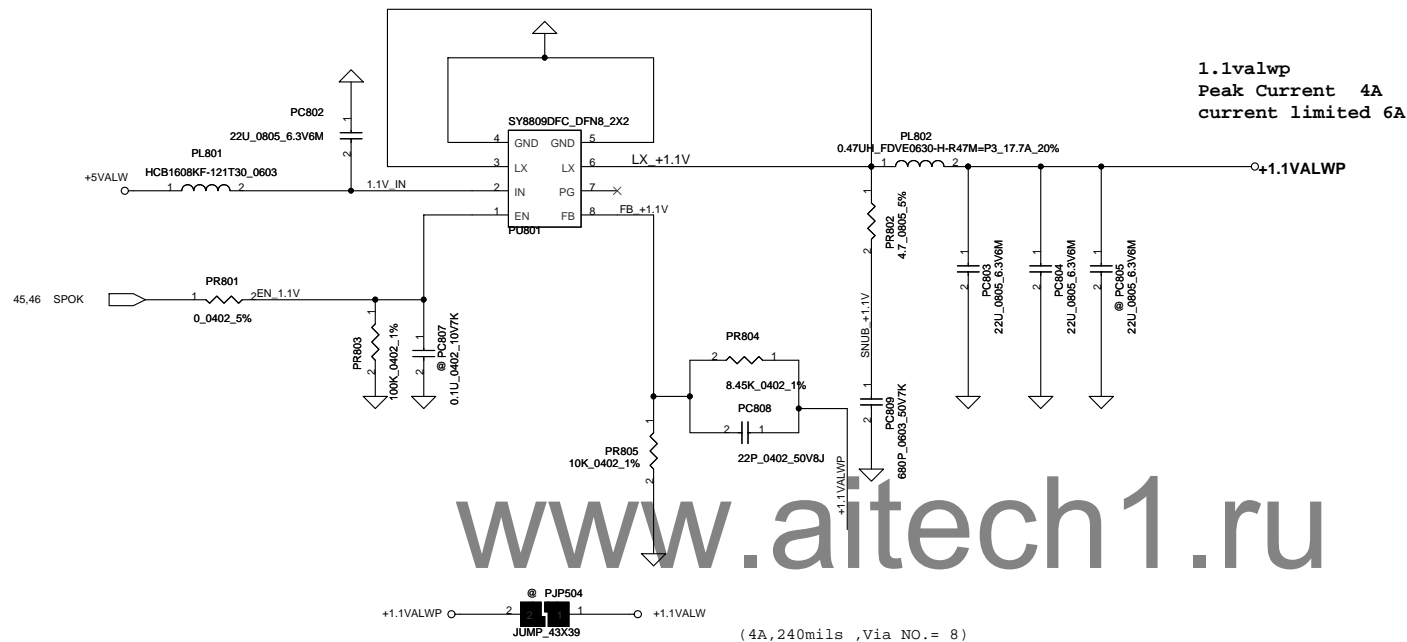
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Vin Detector

	Min.	Typ	Max.
H-->L		17.33V	
L-->H		16.98V	

ILIM and external DPM
4.36A

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				Date:	Tuesday, January 10, 2012
				Sheet	47 of 54



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				Sheet	48 of 54

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SCHEMATICS, MB A8714

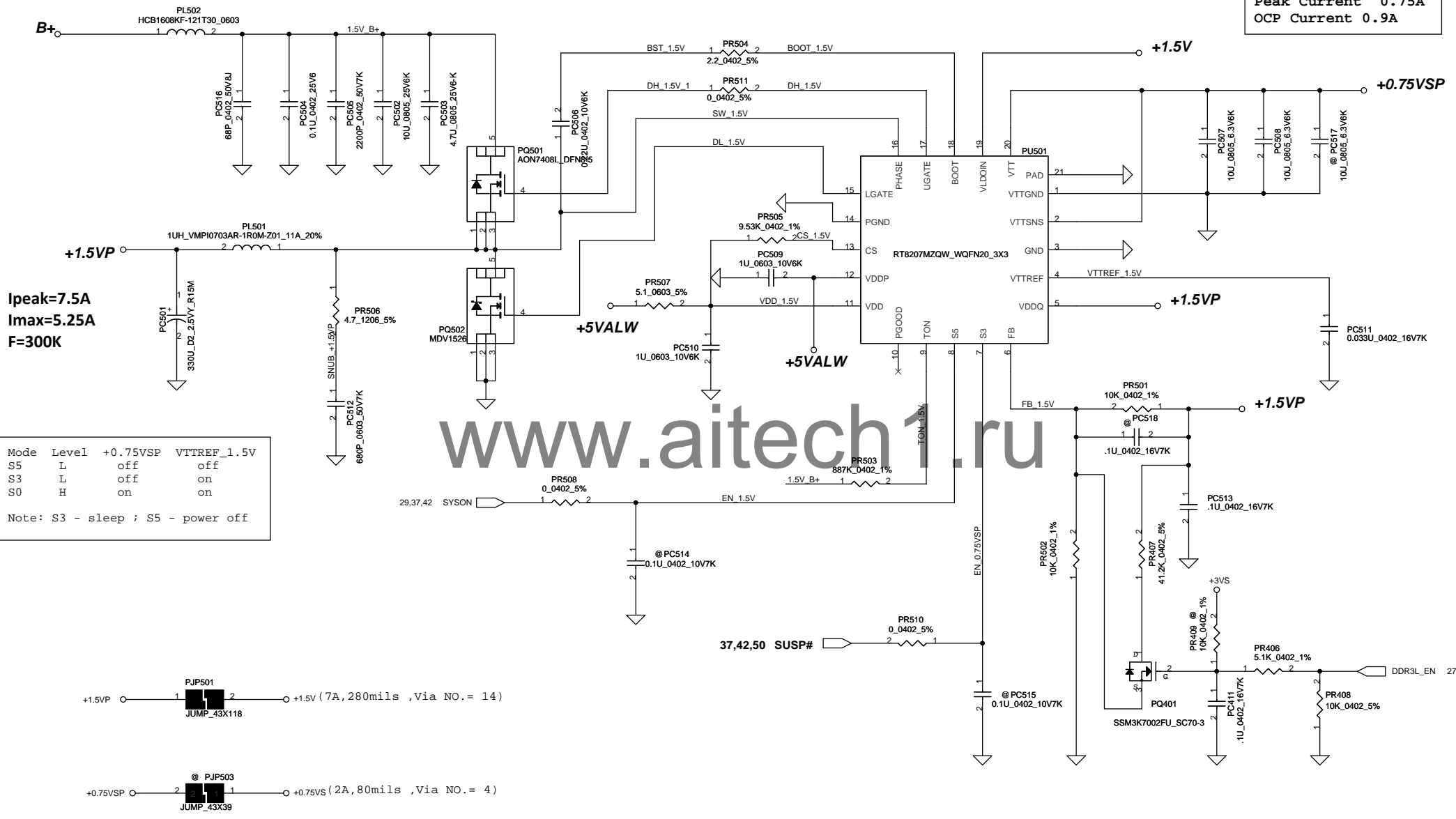
Rev A

I_{peak}=7.5A
I_{max}=5.25A
F=300K

Mode	Level	+0.75VSP	VTTREF_1.5V
S5	L	off	off
S3	L	off	off
S0	H	on	on

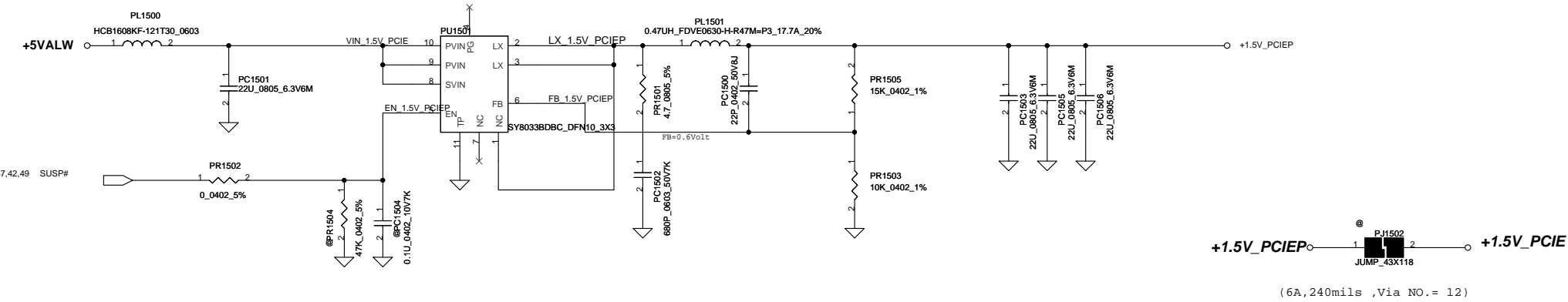
Note: S3 - sleep ; S5 - power off

0.75V_{olt} +/- 5%
TDC 0.525A
Peak Current 0.75A
OCP Current 0.9A



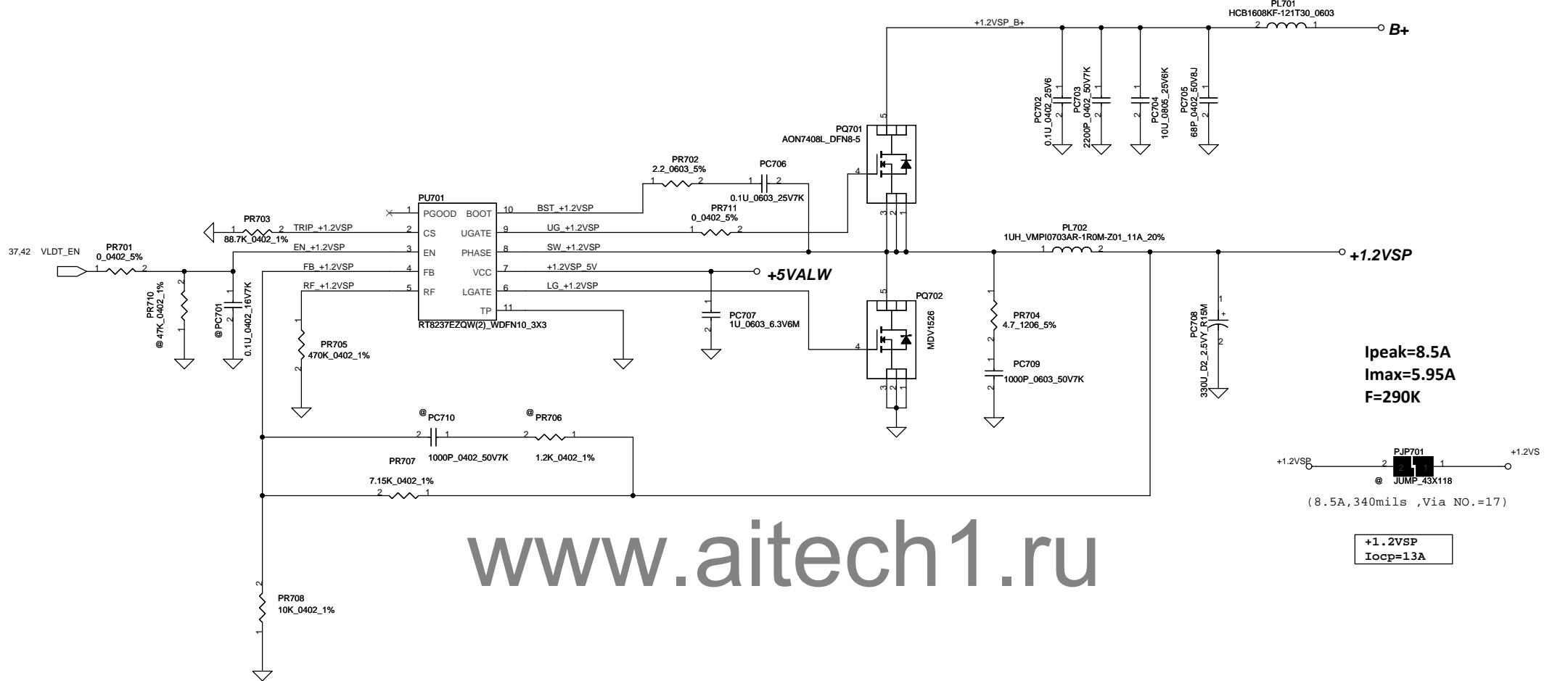
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2011/07/29				2012/07/29				Title			
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Date:				Tuesday, January 10, 2012				Sheet 49 of 54			

1.5VPCIEP
Peak Current 6A
OCP current 6A

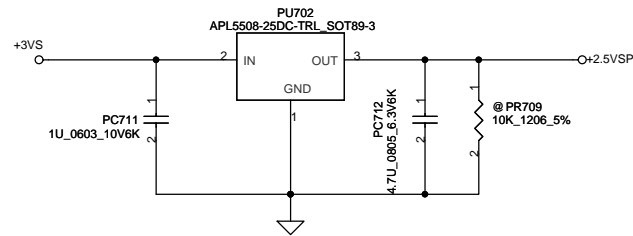


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				Date:	Tuesday, January 10, 2012
				Sheet	50 of 54
				Rev	A

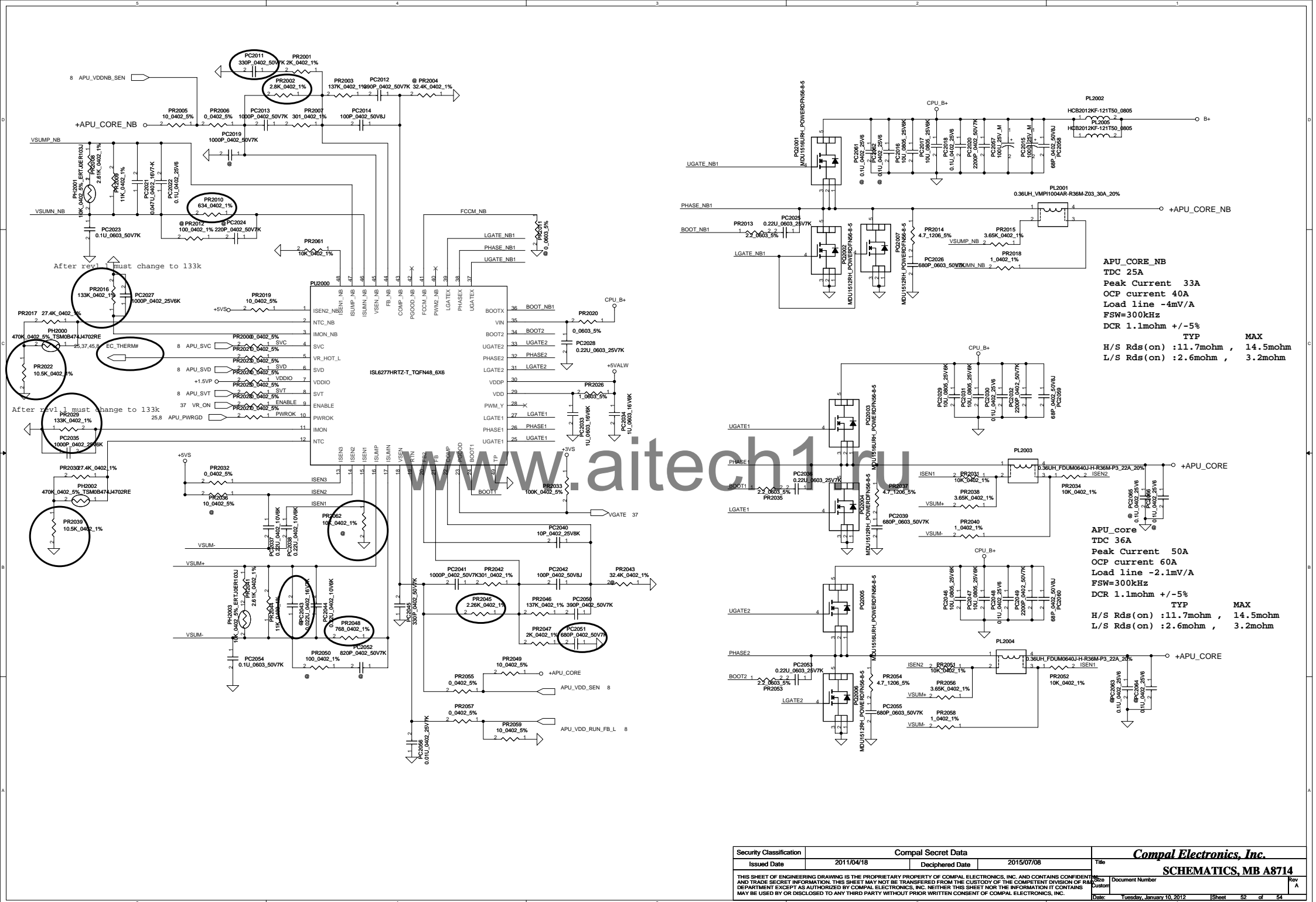


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PJP702
@ JUMP 43X39
(0.75A, 40mils, Via NO.=22)

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			LA-8712P	Rev A
			Date: Tuesday, January 10, 2012	Sheet 51 of 54



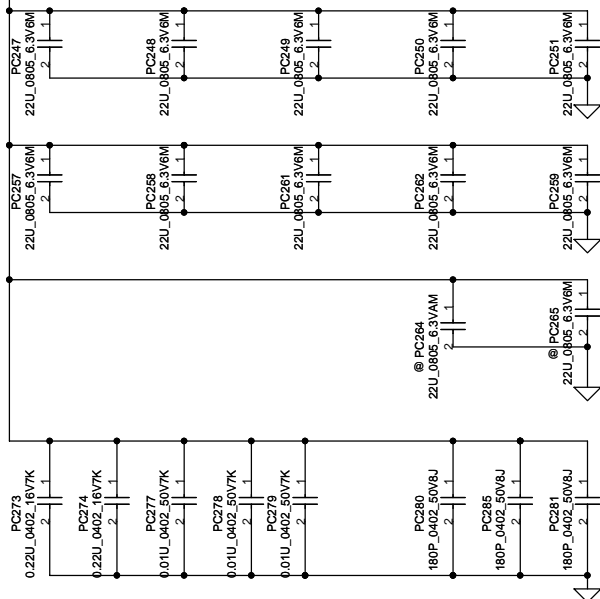
APU_CORE_NB
TDC 25A
Peak Current 33A
OCP current 40A
Load line -4mV/A
FSW=300KHz
DCR 1.1mohm +/-5%
H/S Rds(on) : 11.7mohm , 14.5mohm (TYP, MAX)
L/S Rds(on) : 2.6mohm , 3.2mohm

APU_core
TDC 36A
Peak Current 50A
OCP current 60A
Load line -2.1mV/A
FSW=300KHz
DCR 1.1mohm +/-5%
H/S Rds(on) : 11.7mohm , 14.5mohm (TYP, MAX)
L/S Rds(on) : 2.6mohm , 3.2mohm

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Document Number	Custom	Rev	A	Sheet	82 of 54
Date	Tuesday, January 10, 2012	Sheet	82	of	54

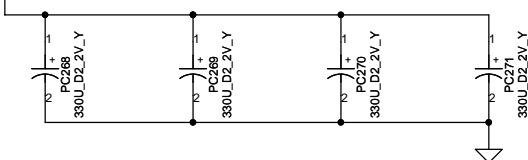
+APU_CORE

+APU_CORE



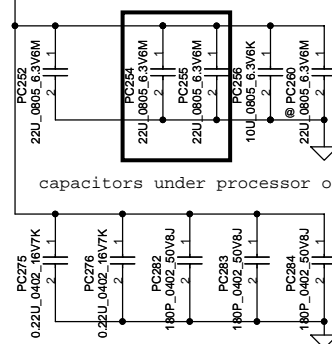
+APU_CORE

Local



+APU_CORE_NB

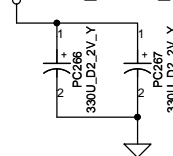
+APU_CORE_NB



capacitors under processor on bottom side of board

+APU_CORE_NB

Local



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				Date	Tuesday, January 10, 2012
				Sheet	53 of 54
				Rev	A

DB-2(12/2)	P44-PWR-DCIN / Vin Detector	Change to PJP1 pine define	DC-IN jack buy and sale define does not change
DB-2(12/8)	P45-PWR-BATTERY CONN	Pin 7 power source change +3VLP to +3VALW	EC command
DB-2(12/8)	P52-PWR-+1.5VPCIE/0.935V	PC11506 loaction change to PC1156	CIC SMT command
DB-2(12/12)	P52-PWR-+1.5VPCIE/1V	Change PR9352 11.3K to 13.3K (0.935V to 1V)	HW comand
DB-2(12/13)	P50-PWR-1.1VALNP	Add PR803 =10K	SY8809 enbale pin issue

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